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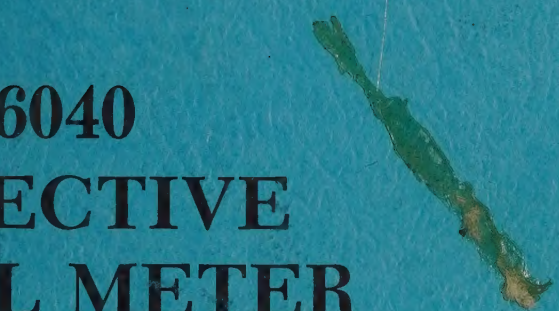
INSTRUCTION MANUAL

6040 SELECTIVE LEVEL METER



RYCOM
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RYCOM INSTRUMENTS INC.
9351 East 59th Street
Raytown, Missouri 64133

INSTRUCTION MANUAL
6040
SELECTIVE LEVEL METER

Serial No. 699

Manual Part No. 030 00030 01

MODEL 6040
FREQUENCY SELECTIVE LEVEL METER

WARRANTY

This instrument is under warranty for one year from date of delivery against defects in material and workmanship (EXCEPTION-BATTERY). We will repair or replace products that prove to be defective during the warranty period. No other warranty is expressed or implied. We are not liable for consequential damages.

FACTORY SERVICE

The Rycom Model 6040 was designed for dependable operation with recommended annual adjustment and calibration. If, however, your 6040 is not working properly, return it to the factory for repair. We recommend that the 6040 be returned in the original containers in which it was received. Send the instrument PREPAID to:

Rycom Instruments, Inc.
9351 E. 59th Street
Raytown, Missouri 64133 U.S.A.
Telephone: 816-353-2100
TWX: 910-771-2182
Answbk: "Rycominstr"

Normally, we will repair and ship back any instrument sent in within 10 days, unless the instrument is unrepairable. In this case, we will advise you.

If you need information, call the Rycom Factory Repair Department at 816-353-2100. If you return your 6040 for service or repair, be sure to include the following information:

1. Name and address of owner.
2. Brief description of symptoms or trouble.

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CHAPTER 1
GENERAL INFORMATION

1.0 INTRODUCTION

This section of the Instruction Manual contains general information and technical specifications for the Rycom Model 6040 Selective Level Meter.

1.1 APPLICATION OF THE INSTRUMENT

The 6040 Selective Level Meter is a portable field or bench instrument designed to make precision measurements of both level and frequency on frequency division multiplex (FDM) equipment baseband signals. The level range of the instrument is −99.9 dBm to 20.9 dBm with 0.1 dB resolution. The frequency range is 300 Hz to 3.5 MHz with a signal counter accuracy of better than 4×10^{-7} in either the 10 Hz fast update mode or the 1 Hz 2 second update mode.

Although its primary application was intended to be on high density long haul microwave systems, the 6040 may be employed on any communications equipment requiring selective level or frequency measurements.

1.2 ELECTRICAL FEATURES

The key electrical features of the 6040 selective level meter are as follows:

- Level Accuracy — ±0.2 dB at carrier frequencies provides the precision required to do end-to-end line-ups on high density, long haul microwave systems. Accurate measurement on the full range of customer test point configurations can be accommodated with the 6040 because this instrument compensates for bridging and impedance errors.
- Auto Level Ranging — is provided to allow the technician to make rapid signal search measurements since the instrument automatically selects the appropriate range for any signal level. The level range may also be manually selected.
- AFC Tuning — automatically takes the tuning errors out of your measurements. The 6040's AFC is locked to the high stability temperature compensated crystal oscillator module so that each measurement is made with the tuning at the same point on the bandpass filter, thus providing repeatable measurement accuracy. The AFC is also a great time-saver since no time consuming manual tuning is required to keep signals in tune. For measurements not suited to AFC tuning such as noise or FSK signals, manual tuning and a high resolution analog tuning indicator are provided.
- Precision Frequency Counter — is built into the 6040 level meter providing the capability of two instruments in one. The precision frequency counter derives its reference from a high stability temperature compensated crystal oscillator module which provides an accuracy of 0.4 ppm. This is excellent for testing the frequency drift on drop and insert carrier channel oscillator and pilots. A signal count with 1 Hz resolution is provided for the measurement of incoming signals. Other frequency display modes provided are signal count with 10 Hz resolution and a center passband frequency; the frequency to which the 6040 is tuned.
- Analog Tuning Meter — In addition to the digital LEVEL dBm display, an analog tuning meter is provided equipped with two ranges. One range provides a 21 dB window for sweeping a baseband for hot signals or observing noise spikes. The second range provides a 4 dB window with an adjustable zero dB set point to make it easy to manually tune and peak a signal with high manual resolution.
- Level Out — A front panel BNC connector provides a linear dBm scaled DC output to drive a recorder or oscilloscope for an analysis of fades, noise or level troubles.
- LCD Digital Displays — of both frequency and level are provided for high visibility. The LCD displays are designed for high ambient temperature operation and are equipped with self regulating heaters for low temperature operaton below 5°C.
- Field Operation — the 6040 weighs 21 lbs and is AC or rechargeable battery powered. It has a unique battery discharge protection feature that helps prevent running out of battery capacity before tests are complete. At a threshold battery voltage, LO BAT alert will flash in the LEVEL dBm display. 25 minutes later, the 6040 shuts itself off to prevent permanent battery damage. By momentarily switching to POWER OFF, the protection circuit can be reset to complete remaining measurements.
- Other Features — Other standard selective level meter electrical features are identified in the Technical Specification Summary of this chapter.

1.3 MECHANICAL FEATURES

The key mechanical features of the 6040 selective level meter are as follows:

- Field Portable — due to compact size, rugged packaging and battery operation. A metal cover protects the front panel of the instrument during transportation. Before the metal cover is installed, the POWER switch must be in the OFF position thus preventing unintentional battery discharge.
- Die Cast Aluminum Front Panel — together with polycarbonate overlay provides great mechanical and electrical stability to the chassis and circuitry and withstands the rigors of shock and vibration experienced in the field.
- Aluminum Chassis, Front Panel and Case — are iridite coated to reduce the corrosion experienced in high humidity conditions. The case and cover are finished with a textured polyurethane enamel to provide an extremely scratch resistant external surface.

1.4 ELECTRICAL DESCRIPTION

The basic 6040 level meter is a selective, dual conversion superheterodyne circuit with auxiliary circuitry to provide the essential power level measurements scaled for signal level and impedance, frequency counting and demodulator functions.

The unit is designed for balanced or unbalanced inputs with 50, 75, 124, 135, 150 or 600 ohm line inputs, terminated or bridging. The front end attenuator circuit employs latching relays for reliable low power switching of level ranges. An AUTO RANGE position on the RANGE dBm (MAX LEVEL) switch permits automatic selection of the proper range for any selected input signal. The wide dynamic range circuitry employed in the 6040 allows accurate measurement of individual signal power levels in telecommunication systems where there are 600 or more channels between 4 kHz and 3.5 MHz; the noise power ratio for an equivalent 600 channel system is better than 55 dB for a 40 dB increase in sensitivity in any band-stopped slot.

The 1st local oscillator is phase locked to provide an AFC capability for ease of tuning. Two bandwidths are provided in the instrument: a narrow filter for measurement of signal carrier levels and a wide filter for signal search and channel level measurements. The standard nominally 3100 Hz wideband filter may be optionally replaced by a C-Message equivalent filter. Similarly, the standard nominally 50 Hz narrowband filter may be optionally replaced by a 100 Hz filter.

A high accuracy and stability frequency counter provides a 6 digit LCD readout of the incoming signal frequency or of the bandpass center frequency to which the level meter is tuned. A

fast updating frequency resolution of 10 Hz is provided which may be changed at will to a 1 Hz resolution with a 2 second update rate.

For locating carriers with no modulation, an audible output on the speaker or headphone is developed by means of a carrier re-insertion oscillator. Either upper or lower sidebands may be selected.

Signal power level is displayed with 0.1 dB resolution on a 3 digit LCD display. ADJUST RANGE lamps flash an alert for signal overload to prevent inaccurate measurements or to indicate the direction of manual level range change for more accurate measurements.

An internal crystal oscillator at a nominal frequency of 250 kHz with a stable level output of −30.0 dBm provides a reference level for calibration of the instrument.

1.5 TECHNICAL SPECIFICATION SUMMARY

1.5.1 Definition

Parameters shown in the following 6040 Selective Level Meter specification summary as being "typical", "nominal" or "approximate" are provided only as non-warranted supplemental information having possible value in the application of the instrument.

1.5.2 Specifications

MODEL	6040
FUNCTION	Selective Level Meter
FREQUENCY	
Range:	
50Ω, 75Ω:—	300 Hz to 3.5 MHz, 50 Hz bandwidth 400 Hz to 3.5 MHz, 100 Hz bandwidth 12.0 kHz to 3.5 MHz, 3.1 kHz, "C" Message bandwidth
124Ω, 135Ω, 150Ω:—	4.0 kHz to 2.0 MHz, 50 Hz, 100 Hz bandwidth 12.0 kHz to 2.0 MHz, 3.1 kHz, "C" Message bandwidth
600Ω:—	300 Hz to 100 kHz, 50 Hz bandwidth 400 Hz to 100 kHz, 100 Hz bandwidth 12.0 kHz to 100 kHz, 3.1 kHz, "C" Message bandwidth
Bands:	Band A — 0.3-650 kHz Band B — 550-1650 kHz Band C — 1300-2400 kHz Band D — 2000-3500 kHz
Signal Counter Accuracy (Initial):	$\pm 4 \times 10^{-7}$ or ±LSD whichever is greater at 23°C after 3 minute warm-up
Signal Counter Accuracy (Long Term):	$\pm 1 \times 10^{-6}$ per year aging rate with reset capability
Temperature Stability:	$\pm 2 \times 10^{-7}$ over the temperature range +20°C to +30°C $\pm 2 \times 10^{-6}$ over the temperature range −10°C to +55°C
Resolution:	Selectable: 10 Hz with fast update, signal count and center passband 1 Hz with 2 second update, signal count only
Display:	6 digit LCD in kHz units
Modes:	Signal Frequency Count with automatic mode switching or Passband Center Frequency Count
Automatic Frequency Control (AFC):	Selectable ON/OFF with either wide or narrow band filter operation
AFC Capture Range:	≥12 dB below RANGE MAX. LEVEL (Frequency range of capture depends on filter employed)

LEVEL

Range: −99.9 dBm to 20.9 dBm

dBm Reference Impedance: Selectable, 50Ω, 75Ω, 124Ω, 135Ω, 150Ω, 600Ω

Ranging: Automatic or manual

Manual Ranges: Eleven switched 10 dB steps

Display: 3 digit LCD with sign

Resolution: 0.1 dB

Level Measurement Accuracy (1):

Range Dependence:—

1. Unbalanced, terminated internally or externally, 75Ω, referred to: 250 kHz, most sensitive manual range for specified level, AFC (ON), 23°C

LEVEL RANGE (dBm)		
−99.9 to −90	−89.9 to 0	0 to +20
±1.0 dB	±0.2 dB	±0.3 dB

2. Unbalanced, terminated internally or externally, 50Ω, 124Ω, 135Ω, 150Ω, referred to: 250 kHz, most sensitive manual range for specified level, AFC (ON), 23°C

   Typically, same as 1. above

3. Unbalanced, terminated internally or externally, 600Ω, referred to: 50 kHz, most sensitive manual range for specified level, AFC (ON), 23°C

   Typically, add ±0.15 dB to 1. above

4. Balanced, terminated internally or externally, 124Ω, referred to: 250 kHz most sensitive manual range for specified level, AFC (ON), 23°C

LEVEL RANGE (dBm)		
−99.9 to −90	−89.9 to 0	0 to +20
±1.0 dB	±0.3 dB	±0.4 dB

5. Balanced, terminated internally or externally, 50Ω, 75Ω, 135Ω, 150Ω, referred to: 250 kHz, most sensitive manual range for specified level, AFC (ON), 23°C

   Typically, same as 4. above

6. Balanced, terminated internally or externally, 600Ω, referred to: 50 kHz, most sensitive manual range for specified level, AFC (ON), 23°C

   Typically, add ±0.15 dB to 4. above

Frequency Dependence:—

1. Unbalanced, terminated internally or externally, 75Ω, referred to: −30 dBm measured on −30 dBm max. level range, AFC (ON), 23°C

FREQUENCY RANGE (kHz)		
0.3 to 12	12 to 3250	3250 to 3500
±0.2 dB	±0.2 dB	+0, −0.5 dB

2. Unbalanced, terminated internally or externally, 50Ω, 124Ω, 135Ω, 150Ω, 600Ω, referred to: −30 dBm measured on −30 dBm MAX. LEVEL range, AFC (ON), 23°C

   Typically, same as 1. above for frequency limits of specified impedance

3. Balanced, terminated internally or externally, 50Ω, 75Ω, 124Ω, 135Ω, 150Ω, 600Ω, referred to: −30 dBm measured on −30 dBm MAX. LEVEL range, AFC (ON), 23°C

   Typically, add ±0.1 dB to 1. above for frequency limits of specified impedance higher than 1.0 kHz. Typically, add ±0.2 dB to 1. above for lower frequency limits of specified impedance 0.3 kHz to 1.0 kHz.

Temperature Dependence:—

1. Without recalibration: ±0.1 dB/°C referred to: 250 kHz, −30 dBm level measured on −30 dBm MAX. LEVEL range at any ambient temperature between −10°C and +55°C, with initial calibration at 23°C
2. With recalibration: See "LEVEL CALIBRATION REFERENCE, Level Stability"

Time Dependence:— See "WARM-UP CHARACTERISTICS"

Analog Peaking Indicator:

Type:— Vertically mounted edgewise meter indicates relative level

Range:— Switchable, typically 20 dB without set point and 4 dB FSD with manual set-point adjustment

Resolution:— Nominally, 1 dB in 20 dB range and 0.2 dB in 4 dB range

Input Over-Range Indicator: Red flashing LED indicator reports over-range signal inputs. Level display is simultaneously blanked

Input Under-Range Indicator: Amber flashing LED indicator reports under-range signal inputs which may cause measurement errors

Maximum Input:

Unbalanced port:— d.c. coupled, +30 dBm bridging or terminated

Balanced ports:— a.c. coupled, +30 dBm bridging or terminated, ±200 V (d.c. and peak a.c.)

WARM-UP CHARACTERISTICS

(Ambient Temperature +23°C, Test Frequency 250 kHz, Filter Wide Band)

Recommended Warm-up Period: 3 minutes

Time Dependent Level Drift
(Initial calibration, no recalibration, input tuning maintained):
3 to 60 minutes ±0.5 dB max.
3 minutes to 4 hours ±0.7 dB max.

Time Dependent Tuning Drift
(Initial tuning, no retuning):

Without AFC:—
3 to 60 minutes ±400 Hz max.
3 minutes to 4 hours ±700 Hz max.

With AFC:—
3 to 60 minutes ±2 Hz max.
3 minutes to 4 hours ±4 Hz max.

LEVEL CALIBRATION REFERENCE

Calibration Level: −30.0 dBm ±0.25 dB at 23°C

Level Stability: Better than ±0.2 dB over operating temperature range (typically ±0.006 dB/°C)

Frequency: 250 kHz ±30 Hz

SELECTIVITY

Wideband Filter: 3100 Hz nominal
Passband: 2 kHz min. at −0.5 dB points
3100Hz ±10% at −3 dB points
Stopband: 9200 Hz max. at −70 dB points

Narrowband Filter:	50 Hz nominal Passband: 20 Hz min. at −0.5 dB points 50 Hz ±10% at −3 dB points Stopband: 365 Hz max. at −70 dB points
INPUT	
Impedance (Balanced):	Terminated — 75Ω, 124Ω, 135Ω, 150Ω, 600Ω Bridging — 50Ω, 75Ω, 124Ω, 135Ω, 150Ω, 600Ω Typically 5 kΩ shunted by 55 pF Automatic level correction with impedance selected Automatic compensation of bridging errors
Impedance (Unbalanced):	Terminated — 75Ω, 124Ω, 135Ω, 150Ω, 600Ω Bridging — 50Ω, 75Ω, 124Ω, 135Ω, 150Ω, 600Ω Typically 5 kΩ shunted by 55 pF Automatic level correction with impedance selected Automatic compensation of bridging errors
Common Mode Rejection:	≥30 dB at 250 kHz ≥20 dB at 1.0 MHz
Return Loss (75Ω Unbalanced):	≥30 dB
Connectors:	
Unbalanced:-	BNC female nom. 75Ω
Balanced:-	Banana jack nom. 600Ω
INTRINSIC DISTORTION	
Noise Power Ratio (NPR) (Equivalent 600 channel system, 75Ω Unbalanced):	≥55 dB for 40 dB increase in sensitivity measured in any band-stopped slot in band
2nd and 3rd Order Harmonics:	≥70 dB below fundamental, single tone 2.5 kHz to 3.5 MHz for 60 dB increase in sensitivity
I.F. and Image Rejection:	≥70 dB
INTERMEDIATE FREQUENCIES	5 MHz and 455 kHz
DEMODULATOR	AM, USB, LSB
OUTPUTS	
Loudspeaker (Internal):	Output greater than 50 milliwatts, adjustable level
External Audio Output:	≥+10 dBm into 600Ω load 5% THD, adjustable level
Harmonic Distortion (1 kHz Tone):	≤5% for 50 milliwatt loudspeaker output
Recorder Output:	Linear dBm scaled output, +4.0 V DC output at RANGE MAX. LEVEL 0.0 V DC at 20 dB below RANGE MAX. LEVEL. Source impedance 2 k ohms
Probe Power Output:	Nominally 12.6 V d.c. 100 ma. max. available at 0.080 in. front panel tip jack
POWER REQUIREMENTS	
AC Supply:	115 V AC ±10%, 50-60 Hz for operation and/or battery charging
Battery Operation:	Internal rechargeable lead acid starved electrolyte battery (See NOTE 2. page 1-6)
Battery Capacity:	Approximately 8 hour normal operation. 6 hour low battery protection cut-off typical. 3 hour operation below 5°C. A discharged battery will recharge overnight
AC Watts:	19 watts with fully charged battery 40 watts with unit operating and battery discharged (operation above 5°C)
Battery Discharge Protection:	25 minutes low voltage advance warning on LCD display. Low voltage battery shut-off, after time-out with manual reset

Powering From External Battery:	12.6 V DC minimum, 2.5 amp maximum to 0.080 in. front panel tip jack
Fuses:	Battery — Type AGA 2 amp A.C. line — Type MDL ¾ amp

MISCELLANEOUS

AC Supply Option:	230 V AC ±10% 50-60 Hz
Standard Filter Options:	
Wideband:—	"C" Message Noise Equivalent Passband: 1,400 Hz min. at −0.5 dB points 2,000 Hz ±10% at −3 dB points Stopband: 6,200 Hz max. at −70 dB points Psophometric Noise Equivalent Passband: 1,740 Hz ±10% at −3 dB points
Narrowband:—	100 Hz nominal Passband: 40 Hz min. at −0.5 dB points 100 Hz ±20% at −3 dB points Stopband: 580 Hz max. at −70 dB points

TEMPERATURE RANGE

Operate:	−10°C to +55°C
Storage:	−40°C to +75°C

MECHANICAL

Dimensions:	8″ x 12″ x 9″ (203.2mm x 304.8mm x 228.6 mm)
Weight:	21 lbs (9.5 kg)

NOTE 1.

Measured after a warm-up period of 30 minutes and after level calibration, unless otherwise noted.

NOTE 2.

The lead acid starved electrolyte battery employed in this unit is sealed and classified as "dry" under International Air Transport Association Restricted Articles Regulation #210. The battery is not subject to Federal hazardous material regulations and is not considered to be a restricted article by the Civil Aviation Authority and the U.S. Department of Transportation. Local governments, however, may have created regional ordinances relating to the disposal of batteries. It is therefore, suggested that a check be made with local authorities before disposal of batteries is made by normal means. In the event that difficulty is experienced, defective batteries may be returned to Rycom for disposal.

CHAPTER 2
OPERATING INSTRUCTIONS

2.0 INTRODUCTION

The various controls, displays, indicators and connectors of the 6040 are shown in Figure 2-1. Identifying numbers correspond to the paragraph suffixes describing these items.

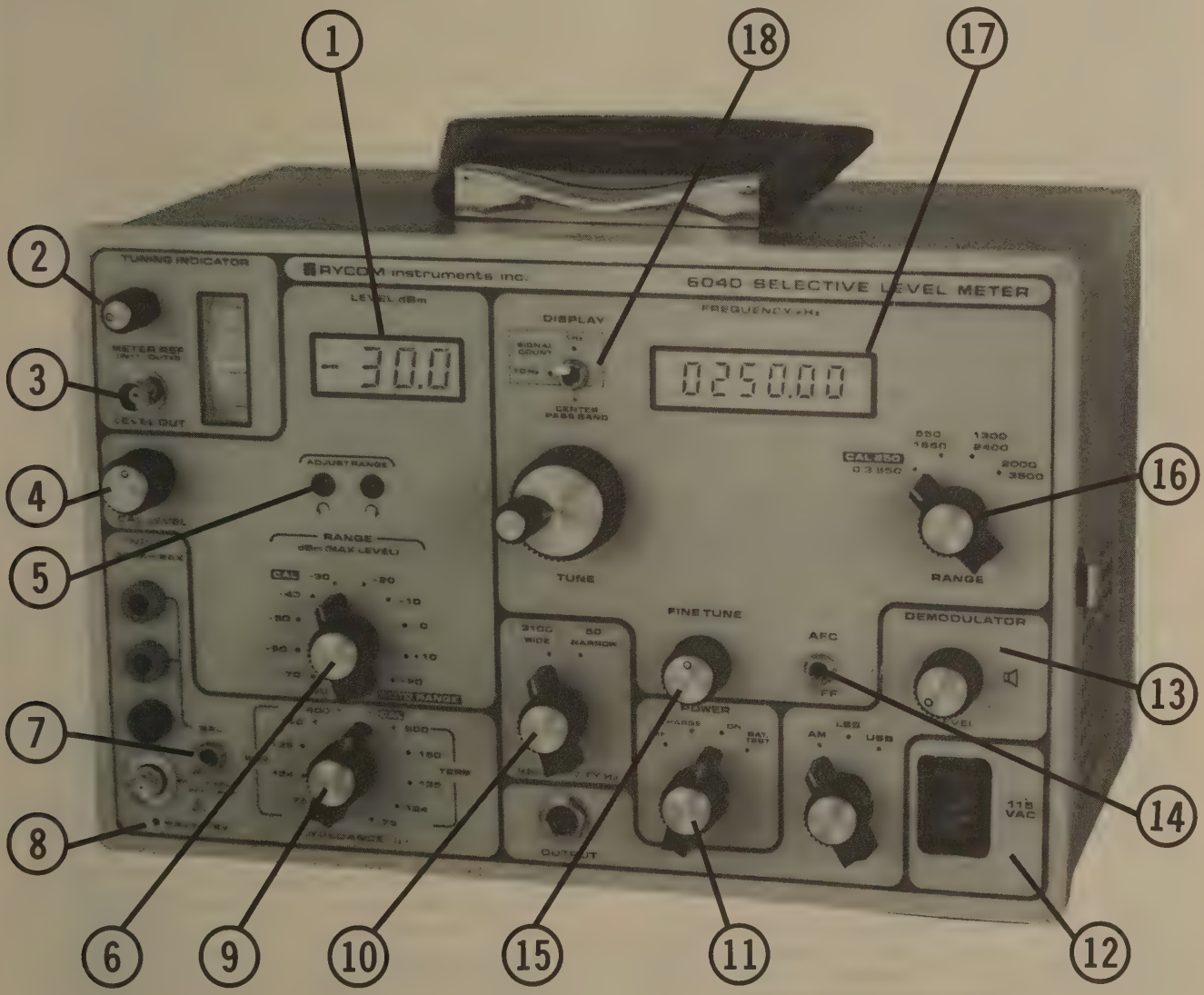


FIGURE 2-1
FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

2.0.1 "LEVEL dBm" Display

The LEVEL display indicates input signal levels with 0.1 dB resolution. The digital LCD display employed is thermostatically controlled, has a rapid display response in the cold and resists damage from heat extremes.

This display also provides a LO BAT alert when the low battery protection circuit is activated. This feature will be described later in Chapter 7.4 POWER.

The level display will blank when the input signal level exceeds the maximum level input shown on the RANGE dBm switch position by greater than +0.9 dB.

2.0.2 "TUNING INDICATOR" Display and Control

The tuning indicator features a two range (4 dB or 21 dB) full scale deflection with an operator adjustable reference level in the lower range provided. Its operation is simultaneous with the digital level display.

With the METER REF control in the (OUTx5) position, the analog TUNING INDICATOR has a full scale range of approximately 4 dB. In this position the reference 0 dB point of the analog TUNING INDICATOR may be adjusted to provide a high analog resolution and sensitivity for the purpose of making gain/level adjustments on users equipment. The resolution is nominally 0.2 dB.

With the METER REF control in the (INx1) position, the analog TUNING INDICATOR has a full scale range of approximately 21 dB. The resolution, in this case, is nominally 1 dB.

2.0.3 "LEVEL OUT" BNC Connector

A DC level output of 5 dB per volt for each attenuator setting is available at the LEVEL OUT BNC connector port. It can be used with an oscilloscope or strip chart recorder for long term analysis of signal level fades or noise conditions. This is a linear dB scaled output with +4 V DC at range reference level and 0.0 V DC at 20 dB below range reference level.

2.0.4 "CAL LEVEL" Control

This potentiometer control allows you to calibrate the level reading of the instrument by adjusting the I.F. gain precisely. The actual calibration procedure is detailed in section 2.1 at the end of this chapter.

2.0.5 "ADJUST RANGE" Indicators

These lamps flash to indicate the direction in which you must manually change level ranges for measurement accuracy. The appropriate direction in which the range switch must be turned is indicated beneath each light. In the AUTO RANGE condition, the lamps indicate the direction in which the range adjustment is being automatically made.

When the 6040 is connected to a signal having a level above the selected level range the red lamp will flash and in addition, the LEVEL dBm display will blank. A signal level above +30 dBm may cause a front end overload and damage the instrument.

2.0.6 "RANGE dBm (MAX LEVEL)" Control

For optimum measurement accuracy when manually setting range levels, the instrument should be operated in the range where the ADJUST RANGE lamps are not flashing. The maximum signal level of each range selection is appropriately marked beside each switch position.

When the AUTO RANGE mode has been selected, the instrument will automatically switch to the proper level range required by the signal across the input terminals.

2.0.7 "BAL UNBAL" Switch

This switch selects the blue banana jacks, or the BNC connector as the operator defined signal input port.

In the UNBAL position, the BNC connector provides an unbalanced input to the unit. The banana jacks are disconnected in this mode and the BNC shield will be connected to case ground. Note that the case will be connected to earth ground when the unit is grounded through a three terminal AC power line cord or by some other earth ground connection.

With the switch in the BAL position, the two blue banana jacks provide a balanced input to the unit. The BNC center conductor in this case will be disconnected.

The black banana jack provides a low impedance point for the connection of the case to a ground of the operators choice.

It is important to note that whenever the banana jacks are employed to make an unbalanced measurement, the BAL UNBAL switch must be placed in the BAL position. The signal should be connected to the upper blue jack for optimum accuracy. The lower blue jack should be connected to signal ground. See figure 2-2 below for a simplified schematic of the configuration of the 6040 input circuitry.

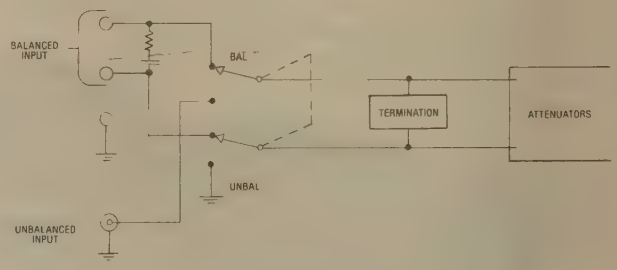


FIGURE 2-2
INPUT CIRCUITRY

2.0.8 "AUX +12V" Connector

This 0.080 inch tip jack connector, in conjunction with the black banana plug socket ground, provides for the possible operation of the selective level meter from an auxiliary 12 V DC battery power source such as an auto battery. Positive connection is made to the tip jack connector. This connector also makes possible the powering of an external probe or other equipment drawing less than 100 mA of current.

2.0.9 "IMPEDANCE (Ω)" Switch

When the switch is set to select a bridging impedance, the input terminals present a high impedance to the line and the LEVEL dBm display is appropriately scaled to reflect the correct power level for the input reference impedance selected. With the switch selecting a terminating impedance, the input terminals are terminated by the line impedance selected and the correct terminated power is shown on the LEVEL dBm display.

For either balanced or unbalanced measurements it is important that the impedance chosen be correctly matched to that of the line on which the measurement is being made.

2.0.10 "SELECTIVITY Hz" Switch

This switch allows you to select the WIDE or NARROW band pass filter suitable for your particular measurements.

2.0.11 "POWER" Switch

A four position "POWER" switch is provided which performs the following functions:

OFF — The instrument should be shut OFF for storage or transportation. A bracket on the face plate cover will prevent the face plate cover from being attached to the instrument unless the instrument is turned "OFF". This prevents the instrument from being left on during transport which will run down the battery.

CHARGE — The internal battery will normally recharge overnight with the switch in this position and be ready for another 8 hours of normal operation.

ON — This position switches the instrument ON for operation for either AC or battery power. When AC is connected to the instrument, the battery will be trickle charged.

BAT. TEST — The battery charge status is shown by a TUNING INDICATOR reading in the section marked BAT OK whenever the switch is in the BAT. TEST position.

A protection circuit will help prevent you from running out of battery capacity before you have completed your measurements and prevent battery damage resulting from over-discharging the battery. When the battery voltage reaches a threshold level, a "LO BAT" alert flashes in the LEVEL dBm display. Exactly 25 minutes after this alert signal, the instrument will shut itself off. The battery protection feature can be reset to allow additional operation of the instrument by momentarily switching the POWER switch to the CHARGE position. Note that, over-use of the reset feature will eventually lead to the deep discharge of the battery and the possible reduction of its life that the protection feature is intended to avoid. It is good practice to restrict use of the reset mechanism to emergency extended operation of the selective level meter.

2.0.12 "115 VAC or 230 VAC" Connector and Line Fuses

This connector mates with the standard line power cable supplied for AC operation of the instrument.

The AC line is protected with a fuse type MDL 3/8 amp.

The battery is also protected with a fuse type AGA 2 amp.

See paragraph 8.2.1 for fuse replacement instructions.

2.0.13 "DEMODULATOR LEVEL" Control and Switch

The DEMODULATOR LEVEL control adjusts the audio level of the speaker and the 600 ohm headset OUTPUT.

The DEMODULATOR switch selects AM or upper (USB) or lower (LSB) single sideband demodulation.

2.0.14 "AFC (Automatic Frequency Control)" Switch

When this switch is in the AFC position, the instrument automatically tunes a signal to the same point on the filter with each measurement. This ensures amplitude accuracy by reducing tuning errors. In order to rapidly tune in the signal, place the SELECTIVITY switch in the WIDE filter position and tune in the signal. Next, switch on the AFC and change to a NARROW filter selection.

Operation of the AFC circuit will provide an AFC indication displayed in the right hand side of the FREQUENCY kHz display window.

Rapidly changing frequency signals such as noise and FSK are not suited to AFC tuning. The AFC should be switched off when making measurements on these signals.

2.0.15 "TUNE/FINE TUNE" Controls

The "TUNE" control provides for coarse/rapid tuning of the frequency band selected. In conjunction with the WIDE filter this control allows for easy location of the desired signal.

The "FINE TUNE" control provides for fine/slow tuning of the frequency band selected. In conjunction with the NARROW filter the FINE TUNE control allows accurate placement of the signal at the desired point in the passband of the filter.

2.0.16 "RANGE" Switch

The RANGE switch sets the frequency range of the instrument to the signal being measured.

Four ranges are provided to cover input frequencies of 0.3 to 3500 kHz.

2.0.17 "FREQUENCY kHz" Display

The 6 digit LCD display shows the frequency of the incoming signal or the frequency to which the instrument is tuned in kHz. The display is thermostatically controlled, resistant to damage from heat and has a rapid response in cold environments.

When the instrument is operating as a frequency counter, a "SIGNAL COUNT" display will appear in the left hand side of the FREQUENCY kHz display.

When the AFC is activated, an "AFC" display will appear in the right hand side of the FREQUENCY kHz display.

2.0.18 "DISPLAY" Switch

This 3 position switch performs the following functions:

CENTER PASS BAND — In this position, the FREQUENCY kHz display will show the frequency to which the instrument is tuned with 10 Hz resolution.

SIGNAL COUNT 10 Hz — In this position, the FREQUENCY kHz display will show the frequency of the incoming signal with 10 Hz resolution. The display will revert back to showing the CENTER PASS BAND frequency when no signal of sufficient strength falls within the filter passband.

SIGNAL COUNT 1 Hz — When the switch is in this position, the FREQUENCY kHz display shows the frequency of the incoming signals to a resolution of 1 Hz. The 1 Hz switch position is spring-loaded and must be momentarily moved into the 1 Hz position when a 1 Hz resolution frequency count display is required. The 1 Hz count will appear after a brief delay following the switch position change. In the SIGNAL COUNT 1 Hz mode, the MHz digit rolls off the display.

2.1 CALIBRATION PROCEDURE

Set the instrument switches and controls as follows:

Switch/Control	Position
RANGE dBm	CAL −30
IMPEDANCE	CAL
SELECTIVITY Hz	Band Pass Filter which you intend to use to make your measurement.
AFC	ON
RANGE kHz	CAL 250, 0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

Note that the CAL positions on the various controls are clearly marked in negative image letters.

To calibrate, adjust the CAL LEVEL to −30.0 dBm on the LEVEL dBm display.

For maximum level accuracy, always calibrate the instrument with the band pass filter that you intend to use to make your measurements.

Usually, only a three minute warmup period is required before you may accurately calibrate and operate the 6040. When turning on the instrument in extreme cold or hot conditions, a slightly longer warmup may be required. For the most accurate measurements, recalibration every 15 to 20 minutes within the first 60 minutes of operation is recommended, particularly when the instrument has been moved from one environmental extreme to another.

CHAPTER 3
THEORY OF OPERATION

3.0 GENERAL

Chapter 3 provides an overall description of the 6040 operation. A detailed explanation of the operation of the major circuit blocks will be provided in chapters 4, 5, 6, and 7.

3.1 UNIT BLOCK DIAGRAM

A simplified block diagram of the unit is shown in figure 3-1. Dashed lines divide the blocks into four groups identified by chapter numbers which refer to the specific chapter which contains the more detailed explanation of the particular block to be studied. Additional block diagrams will be found in these chapters delineating particular circuit functions.

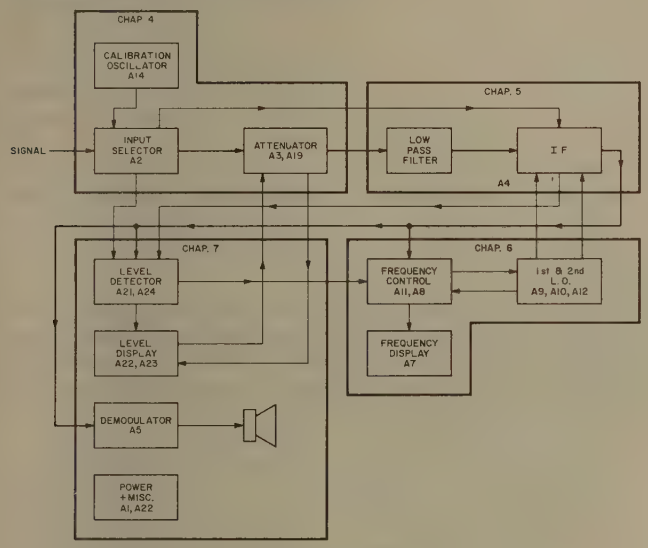


FIGURE 3-1
6040 SIMPLIFIED
FUNCTIONAL DIAGRAM

3.2 INPUT SELECTOR and CALIBRATION OSCILLATOR

The input selector block contains the IMPEDANCE and BAL-UNBAL switches. These switches select the source of the input signal and adjust the termination resistance to be provided at the unit input. With the IMPEDANCE switch in the CAL position the signal source is derived from the calibration oscillator permitting the unit gain to be set to establish the level accuracy. The calibration oscillator operates at approximately 250 kHz and provides a signal source of −30 dBm 75 ohm level to the unit.

The various positions of the IMPEDANCE switch provide information to the I.F. and level detector blocks regarding the input configuration and reference impedance selected.

The position of the BAL-UNBAL toggle switch connects either the unbalanced BNC input or the balanced banana jack pair to the unit.

3.3 ATTENUATOR

The attenuator block contains a dual attenuator, auto ranging circuitry and a summing amplifier. When the RANGE dBm switch is not in the AUTO RANGE position, the attenuation may be adjusted in 10 dB steps by this switch. Each attenuator provides a total attenuation of 100 dB per input leg of the balanced input terminals when the RANGE dBm switch is in the +20 dBm position.

The auto ranging circuitry receives signals from the level display block indicating whether the output from the I.F. block is above or below the required level needed to generate a valid level display. When the auto ranging is enabled, the auto ranging circuitry increments or decrements the attenuation as prescribed by the level display signals. The two balanced attenuator outputs are combined by a summing amplifier to provide a single-ended signal to the lowpass filter.

3.4 LOWPASS FILTER and I.F.

The lowpass filter limits the bandwidth of the signal provided to the I.F. and eliminates undesirable image responses due to high frequency signals appearing in the output.

The I.F. block contains all the elements of a dual conversion superheterodyne circuit. The lowpass filter output is buffered and then mixed with the 1st L.O. signal generating a 5.0 MHz 1st I.F. signal. This 5.0 MHz signal is bandpass filtered by a filter which controls the bandwidth when the SELECTIVITY is in the WIDE position.

The output of this first wide filter is amplified and fed to a 2nd mixer. The 2nd mixer in turn mixes the 5.0 MHz signal with the 2nd L.O. signal (4,545.0 kHz) to generate a 455 kHz 2nd I.F. signal. The buffered output of the 2nd mixer drives gain fixing circuitry. Resistance networks and a multiplexing I.C. permit digital signals from the input selector block to control I.F. gain in accordance with the position of the IMPEDANCE switch.

Between stages of the 455 kHz amplification is a pair of filters. The position of the SELECTIVITY switch determines whether the 455 kHz signal passes through the NARROW filter establishing the NARROW selectivity bandwidth or through the WIDE 10 kHz bandwidth filter. With the WIDE 455 kHz filter selected, the bandwidth is determined by the 5.0 MHz filter referred to above.

A low impedance I.F. output stage drives inputs to the frequency control, level detector and demodulator blocks.

The SELECTIVITY switch also controls circuitry which performs noise compensation appropriate to the selected bandwidth.

3.5 FREQUENCY BLOCKS

The frequency control block contains an accurate TCXO. This oscillator provides a precision time base for frequency counting and a clock signal for analog signal to dBm conversion.

Two phase lock loops are contained within the frequency control block. The reference signals for both loops are derived by dividing down the TCXO frequency. One loop maintains the 2nd L.O. at a 4,545,000.0 Hz frequency and remains locked at all times. The 2nd (AFC) loop is activated in the AFC mode and controls the 1st L.O.. This 2nd loop controls the 1st L.O. in such a manner that the 2nd I.F. frequency is held at 455 kHz. Having a 2nd L.O. locked at 4,545,000.0 Hz and a 2nd I.F. output locked at 455 kHz establishes a 1st I.F. that is, in turn, locked at 5.0 MHz.

The frequency control block also contains frequency subtractor circuits used to provide a count input to the frequency display. When operating in a signal count mode, the 2nd I.F. signal is subtracted from the difference signal derived from 1st and 2nd L.O. signals. This process regenerates the input frequency:

$$F_{in} = (F_{1st\ LO} - F_{2nd\ LO}) - F_{2nd\ IF}$$

When operating in the CENTER PASS BAND display mode the 2nd I.F. signal is replaced by a signal derived from the TCXO.

Both L.O.'s supply signals to the I.F. for mixing purposes and also to the frequency control block for count signal generation

and phase locking. Both oscillators are voltage controlled. The 2nd L.O. remains phase locked at a constant 4,545.0 kHz. The 1st L.O. is variable and is tuned by an air variable capacitor, operator adjusted by the large TUNE knob. The FINE TUNE knob adds a voltage component to the 1st L.O. control voltage. When in an AFC mode, the 1st L.O. control voltage adjusts the 1st L.O. to maintain a constant 455.0 kHz 2nd I.F. output frequency.

The frequency display section consists of a counter and decoder driver circuitry to provide an LCD display of the count. For a 10 Hz resolution display the count interval is 1/5 second and the counted signal is 1/2 the frequency of the displayed frequency.

To obtain a 1 Hz resolution display the count interval is extended to 2.0 seconds. The start of a count interval is synchronized with the leading edge of the count signal to reduce least significant digit jitter.

3.6 LEVEL BLOCKS

The level detector block generates a DC voltage which follows the peak value of the I.F. input to that block. The DC voltage is then used to charge a capacitor. The time required to discharge the capacitor through a resistor to a fixed threshold voltage is proportional to the logarithm of the voltage originally applied to the capacitor. The level detector generates pulse outputs whose widths are proportional to the logarithm of the I.F. voltage and therefore, the logarithm of the selected input voltage. In order to generate analog signals for the TUNING INDICATOR and LEVEL OUT functions, the level detector pulse signal is lowpass filtered. These filtered signals have an average DC value proportional to the logarithm of the input signal.

In generating a digital level display, the level detector pulses are used to gate a count input signal to the level display counter. For wider pulses, more counts are accumulated by the level counter. The starting count for a particular level range is determined by signals derived from the attenuator block. Each level reading consists of the sum of the starting count determined by attenuator block signals, plus the count inputs gated to the counter during the period level detector pulses are received.

A second counter with a fixed zero starting count is used to generate the signals that direct the attenuator block to increase or decrease attenuation together with those that control the ADJUST RANGE indicators.

A resistor network controlled by the IMPEDANCE and SELECTIVITY switches determines the amount of level output voltage that is fedback and substracted from the detected DC voltage. This feedback voltage is used to compensate for internal noise added to the detected DC voltage.

3.7 DEMODULATOR

During the AM demodulation mode, the 2nd I.F. signal is shunt detected, lowpass filtered and then amplified by the audio amplifier.

In the LSB or USB mode the carrier injection oscillator operates at either a 453.5 kHz or 456.5 kHz frequency. A shunt demodulator shorts the 455 kHz I.F. signal to ground at the injection frequency. The audio beat frequency generated by the demodulator is amplified by the audio amplifier.

3.8 POWER BLOCKS

The POWER switch has OFF, CHARGE, ON and BAT. TEST positions. With the POWER switch in the CHARGE position and AC power connected, the converted DC power is used only to recharge the battery. The charging voltage remains above 14.7 volts as long as the charging current accepted by the battery remains above 200 mA. As the battery becomes fully charged, the reduction in charging current accepted by the battery switches the charging circuit output voltage to a lower trickle charge value. The charging voltage switching action thus prevents a battery overcharge.

When the POWER switch is in the ON position, power is supplied for operating the unit either from an AC source, or from the battery whenever the AC power is not connected.

With AC power connected, the battery will be trickle charged during unit operation.

Placing the POWER switch in the BAT. TEST position disconnects any AC power at the power input and retains operation on battery power. The TUNING INDICATOR displays the voltage that exists between the battery terminals and one of the regulated DC output lines.

While operating in the ON mode, the battery voltage is monitored by a comparator. When the battery voltage drops below about 11.8 volts, a counter is activated whose function is to provide a time limit to further extended operation of the unit thus preventing a deep discharge condition from occuring. One binary stage of the counter provides a flashing LO BAT indication on the LEVEL dBm display. Power to the unit is supplied through a latching relay. When the LO BAT counter reaches a turn-off count, the power relay is switched to the OFF position. The LO BAT counter takes 25 minutes to reach the turn-off count and may be reset by placing the POWER switch in the CHARGE position.

The POWER block also contains a number of three terminal regulators used to regulate and isolate the power provided to the various blocks of the unit.

CHAPTER 4
THEORY OF OPERATION FOR THE CALIBRATION OSCILLATOR, INPUT SELECTOR AND ATTENUATOR

4.0 GENERAL

The calibration oscillator circuit is located on the A14 circuit board. The input selector circuit is located on the A2 circuit board. The attenuator circuit is located on the A3 and A19 circuit boards. Refer to figure 12-1 for the schematic diagram of the A2, A3, A14, and A19 circuit boards. A block diagram of these boards is shown in figure 4-1.

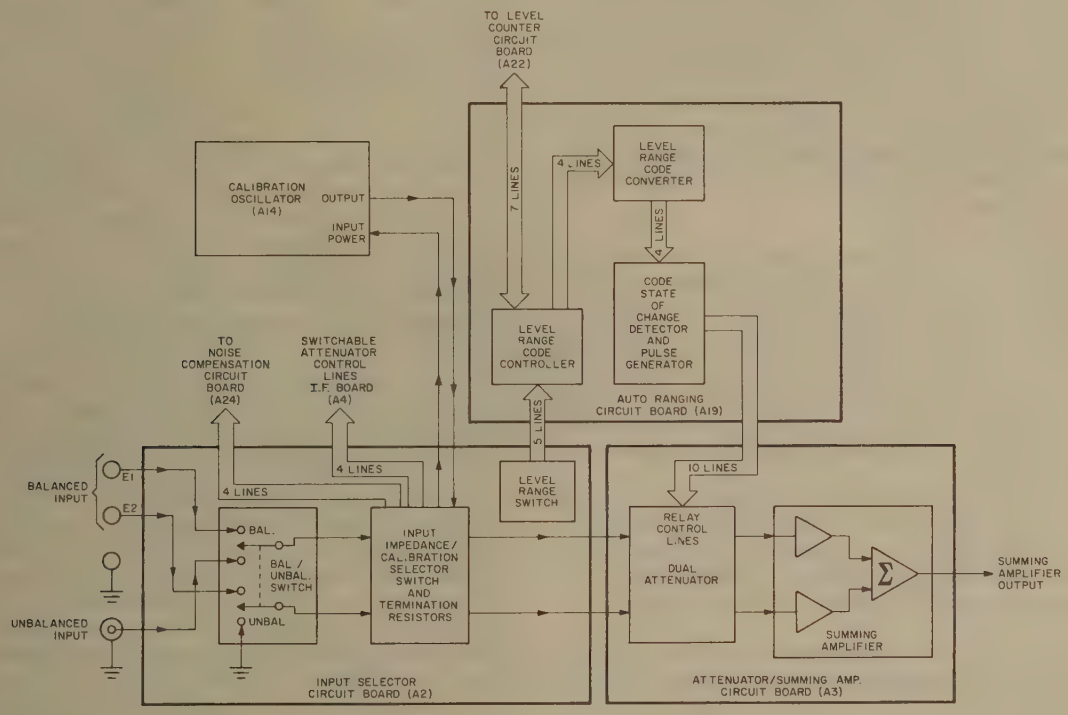


FIGURE 4-1
CALIBRATION OSCILLATOR, INPUT SELECTOR AND ATTENUATOR/SUMMING AMPLIFIER

4.1 CALIBRATION OSCILLATOR

The calibration oscillator circuit board A14 generates an extremely accurate −30.0 dBm reference level signal at 250 kHz; it is used to calibrate the 6040. The oscillator is crystal controlled. Output amplitude stability is achieved by powering the circuit from a precision voltage supply. A 10 V DC regulator A19I13 powers the 6.9 V DC precision voltage reference circuit (A14CR1 and A14R1), whose output is connected to the oscillator circuit. Voltage is supplied to the oscillator only when the IMPEDANCE switch A2S2D is in the CAL position; this avoids possible interference from the calibration signal when measuring input signals near 250 kHz or any of its harmonics. The input terminals of the 6040 are disconnected from the circuit whenever the calibration oscillator is connected.

NOR gate A14I1C is biased in its linear region by feedback resistors A14R2 and A14R3. A 180° output-to-input voltage phase relationship is necessary to sustain oscillations. The 180° phase shift is achieved with two cascaded networks A14R3/A14C2 and A14Y1/A14C1. NOR gates A14I1A and A14I1B are connected in parallel, forming a single inverter whose output switches between +6.9 V DC and ground. An adjustable resistive attenuator A14R5 reduces the 250 kHz frequency component to an output level equivalent to −30.0 dBm into a 75 ohm termination.

4.2 INPUT SELECTOR

The input selector circuit board A2 provides the selection of the following functions:

(a) Permits the selection of a balanced (BAL) or unbalanced (UNBAL) input mode.

(b) The IMPEDANCE switch provides a choice of several bridging (BRG) and terminated (TERM) input impedances, plus the calibration (CAL) mode.

(c) The RANGE dBm (MAX LEVEL) switch allows the selection of several input signal power level ranges (−80 dBm through +20 dBm) and an AUTO RANGE mode.

Switch A2S1A selects either the unbalanced (UNBAL) input signal (BNC jack) or one side of the balanced (BAL) input signal (top blue banana jack E1). The IMPEDANCE switch A2S2A-front selects between the output of switch A2S1A and the calibration oscillator, connecting the selected signal to output jack A2J1 via capacitor A2C3. In the termination (TERM) impedance modes (75, 124, 135, 150 and 600 ohms), switch A2S2A-front connects the corresponding termination resistors A2R1 through A2R10 to the input signal line.

Switch A2S1B selects either signal ground (UNBAL mode) or the other side of the balanced (BAL) signal (center blue banana jack E2). The black banana jack is the common signal ground

connection for balanced input signals. The IMPEDANCE switch A2S2A-rear selects between the output of switch A2S1B (non CAL positions) and the output of switch A2S2D pin 12 (signal ground-CAL position). It connects the selected signal to output jack A2J2 via capacitor A2C2. The selected signal is also connected to the other side of the termination resistors via IMPEDANCE switch A2S1C which makes a DC connection in the UNBAL position and an AC connection through capacitor A2C1 in the BAL position. In the CAL mode, switch A2S2A disconnects the input signal ports from the input circuitry during the calibration procedure.

The A2J1 and A2J2 output jacks on the input selector board are connected to opposite sides of the dual input attenuator. The input impedance of each attenuator half with respect to signal ground is 5,000 ohms. The input impedance measured between both sides of the attenuator (balanced mode) is 10,000 ohms. An unbalanced input signal in the bridging (BRG) mode will see a 5,000 ohm load impedance at the 6040 BNC input jack. In the unbalanced (UNBAL) termination (TERM) mode, this 5,000 ohms is in parallel with the selected termination resistors. The combined internal impedances equal the impedance shown on the IMPEDANCE switch A2S2.

A 10,000 ohm impedance (A2R11 and A2C4) is connected across the two blue banana jacks. This impedance, in parallel with the 10,000 ohm impedance of the dual attenuator, provides a resultant 5,000 ohm input impedance in the balanced (BAL) bridging (BRG) mode. In the balanced (BAL) termination (TERM) mode, this 5,000 ohms is combined with the selected termination resistors to provide a resultant input impedance equal to the impedance shown on the IMPEDANCE switch A2S2.

The 6040 automatically compensates for bridging errors. Any minor voltage loss to the external circuit, which results from the bridging of the 5,000 ohm input impedance across the line, is automatically added back to the measured power level; thus the actual correct power level of the circuit is displayed by the 6040.

The IMPEDANCE switch A2S2B performs switching functions for the noise compensation circuit A24; see chapter 7 for the theory of operation.

The RANGE dBm (MAX LEVEL) switch A2S3 is used to select the front end attenuator range. The AUTO RANGE position allows for the automatic selection of the proper level range. Coded digital information is transferred from this switch to the auto ranging circuit A19 where the data is converted into signals that control the operation of the dual input attenuator.

4.3 ATTENUATOR

The input attenuator circuitry is located on the attenuator/summing amplifier A3 and auto ranging A19 circuit boards.

4.3.1 Attenuator/Summing Amplifier

The attenuator/summing amplifier circuit A3 contains the dual input attenuator and summing amplifier. The output from the two attenuators is fed to the summing amplifier, converting the balanced or unbalanced signals into a single unbalanced output signal.

The two output jacks A2J1 and A2J2 on the input selector board are connected to the dual input attenuator via coaxial cables W1/P1 and W2/P2. Both attenuators are identical in operation. Each attenuator consists of four cascaded voltage divider sections (pads) which are individually switched "in" or "out" of the circuit with latching relays A3K1, A3K2, A3K3 and A3K4. Each of the four relays simultaneously switch identical pads in both attenuators. Each attenuator consists of two 40 dB pads, followed by a 20 dB pad and a 10 dB pad. Because each pad has the same input impedance (5,000 ohms) when its output is terminated with 5,000 ohms, any combination of pads may be switched "in" or "out" without loss of accuracy due to impedance mismatch. The outputs of both attenuators are fed to the two summing amplifier inputs which have 5,000 ohm input impedances. Latching pulses are transmitted by the auto ranging board A19 to switch the relays to their proper "in" or "out" positions.

The summing amplifier combines the two output signals from the dual input attenuator into a single unbalanced output signal. Input signals that are 180° out-of-phase are added together. Signals that are in-phase are algebraically subtracted or cancelled. The signal originating at the unbalanced BNC or E1 banana jack is coupled to the base of A3Q1A pin 2, an emitter follower amplifier. The output of A3Q1A (emitter pin 3) is connected to an active current source (A3Q1D and associated circuitry) which lowers the amplifier distortion for large input signal voltage swings. This output is also connected to the base of A3Q2, an emitter follower amplifier. The signal originating at the E2 banana jack (ground in the unbalanced (UNBAL) mode) is coupled to the base of A3Q1B pin 6, an emitter follower amplifier. The output of A3Q1B (emitter pin 5) is connected to an active current source (A3Q1C and associated circuitry) and to the base of A3Q3, an emitter follower amplifier.

The actual summing of the two signals occurs in the common emitter circuit of A3Q2 and A3Q3; the emitter current flowing in both amplifiers is equal to the difference between the two emitter voltages divided by the resistance A3R26 between them. An increasing signal voltage at the base of A3Q2 will cause an equivalent increase in the voltage drop across A3R26. Conversely, an increasing signal voltage at the base of A3Q3 will cause an equivalent decrease in the voltage drop across A3R26. The fluctuating voltage drop across A3R26 will cause proportional changes in the collector current of A3Q3, thus developing a corresponding output signal voltage across A3R36. The A3C15 capacitance adjustment is used to balance the gain/frequency-response characteristics of both sides of the summing amplifier. This optimizes the common mode rejection for a balanced input signal. The output coax cable W3/P3 is connected to the lowpass filter on the I.F. circuit board A4.

4.3.2 Auto Ranging

The auto ranging circuit board is composed of three major sub-blocks:

(a) Level range code controller
(b) Level range code converter
(c) Code state-of-change detector and pulse generator

4.3.2.1 Level Range Code Controller

The RANGE dBm (MAX LEVEL) switch A2S3 is connected to the auto ranging circuit A19 via the A2J3/A3P1 right-angle connector set. This switch selectively grounds code lines A, B, C, D, and E. Pull-up resistors A19R1 through A19R5 and debounce capacitors A19C1 through A19C5 are connected to these code lines. The truth table for the switch outputs is shown in table 4-1. Input lines C (A19P1 pin 5) and E (A19P1 pin 3) are both connected to a 2-input OR gate A19I4A; the output line C1 replaces both input lines. The truth table for code lines A, B, C1 and D is shown in table 4-2. The hexadecimal equivalent has been included for convenience.

TABLE 4-1
AUTO RANGING INPUT CODES

RANGE dBm (MAX LEVEL) SWITCH (A2S3) POSITION	A19P1				
	PIN 3 E	PIN 8 D	PIN 5 C	PIN 7 B	PIN 4 A
−80 dBm	0	1	0	0	1
−70 dBm	0	1	0	0	0
−60 dBm	0	0	1	1	1
−50 dBm	0	0	1	1	0
−40 dBm	0	0	1	0	1
−30 dBm	0	0	1	0	0
−20 dBm	0	0	0	1	1
−10 dBm	0	0	0	1	0
0 dBm	0	0	0	0	1
+10 dBm	0	0	0	0	0
+20 dBm	1	1	0	1	1
AUTO RANGE	1	1	0	1	0

TABLE 4-2
MODIFIED AUTO RANGING INPUT CODES

RANGE dBm (MAX LEVEL) SWITCH (A2S3) POSITION	CODE LINES				FOUR LINE HEX CODE
	A19I5 PIN 1 D	A19I1 PIN 13 C1	A19I1 PIN 12 B	A19I1 PIN 4 A	
−80 dBm	1	0	0	1	9
−70 dBm	1	0	0	0	8
−60 dBm	0	1	1	1	7
−50 dBm	0	1	1	0	6
−40 dBm	0	1	0	1	5
−30 dBm	0	1	0	0	4
−20 dBm	0	0	1	1	3
−10 dBm	0	0	1	0	2
0 dBm	0	0	0	1	1
+10 dBm	0	0	0	0	0
+20 dBm	1	1	1	1	F
AUTO RANGE	1	1	1	0	E

The 4-input AND gate A19I3B decodes the auto range mode code 1110 from code lines A, B, C1 and D. The A code line is inverted by A19I2F so that A19I3B simply decodes the 1111 state at its input and gives a corresponding high (1) output. The output of A19I3B is inverted by A19I2A. The output of A19I2A is connected to A19I5A pin 2 and A19I4B pin 5. A19I5A acts as a non-inverting buffer in the non-auto range mode allowing code lines A, B, C1 and D to be directly connected to the jam (data) inputs J0, J1, J2 and J3 of the binary up/down counter A19I1. A19I5A turns off (0) in the auto range mode, forcing a jam input code of 0110 to A19I1. In the non-auto range mode, A19I4B is forced to a high (1) output state; this output signal is transmitted through the non-inverting glitch swallower circuit A19I6 (explained later in this section) to the preset enable input of the counter A19I1 pin 1. The high (1) input level to the counter preset enable forces the binary counter outputs Q0, Q1, Q2 and Q3 to be constantly preset to the jam input codes A, B, C1 and D. When the RANGE dBm (MAX LEVEL) switch is moved to the AUTO RANGE position, the 0110 jam input code appears at the inputs of A19I1 one CMOS propagation delay in advance of the preset enable line going low (0) and locks out further jam input code changes. With the preset enable line low (0), the internal binary counters are enabled for up/down counting as dictated by the auto ranging control circuitry.

The four A19I1 counter outputs Q0, Q1, Q2 and Q3 are connected to A19I3A (4 input AND gate) which decodes the 1111 state (+20 dBm) and gives a corresponding high (1) output. The output is connected to A19J1 pin 4, the E line output signal. The E line also connects to one input each of the four dual-input XOR gates A19I8; this converts the remaining four inputs of A19I8 into buffers that are non-inverting when E is low (0) and inverting when E is high (1). The four A19I1 counter outputs Q0, Q1, Q2 and Q3 are connected to the four A19I8 buffers. The outputs of A19I8 are connected to A19J1. The truth table for the A19J1 outputs is shown in table 4-3.

TABLE 4-3
AUTO RANGING OUTPUT CODES TO LEVEL COUNTER CIRCUIT

LEVEL RANGE ATTENUATOR POSITION	A19J1				
	PIN 4 E	PIN 8 D	PIN 3 C	PIN 2 B	PIN 1 A
−80 dBm	0	1	0	0	1
−70 dBm	0	1	0	0	0
−60 dBm	0	0	1	1	1
−50 dBm	0	0	1	1	0
−40 dBm	0	0	1	0	1
−30 dBm	0	0	1	0	0
−20 dBm	0	0	0	1	1
−10 dBm	0	0	0	1	0
0 dBm	0	0	0	0	1
+10 dBm	0	0	0	0	0
+20 dBm	1	0	0	0	0

When the 6040 level range (manual or auto range) is incorrectly matched to the input signal level, the level counter circuit A22 will try to correct the input attenuator level range by telling the auto ranging counter A19I1 which direction to count (up (0), down (1)) and when to count (clock). In the manual mode, the counter A19I1 ignores the update signals from the level counter circuit A22, because the preset enable line A19I1 pin 1 is high (1). When the preset enable line goes low (auto range mode), the counter responds to the up/down and clock signals. Control logic has been included so that the counter cannot count up beyond 1001 or down below 1111. A19I3A decodes the 1111 state. The output of A19I3A is ANDed at A19I5B with the up/down line A19J1 pin 6. When both input signals to A19I5B are high (1), a high (1) output signal is transmitted to A19I4C and then to A19I1 pin 5 which inhibits the counter. As long as the up/down line remains high (1), the counter will remain in state 1111. When the up/down line goes low (0) again, the signal to A19I1 pin 5 also goes low (0) and counting may be resumed in the "up" direction. A19I7A and A19I5D decode the 1001 state. The output of A19I5D is ANDed at A19I5C with the up/down line that has been inverted by A19I7C. In the 1001 state, the counter is inhibited as long as the up/down line remains low (0). When it goes high (1) again, counting may be resumed in the down direction. At any valid code between 1001 and 1111 (excluding 1010, 1011, 1100, 1101 and 1110), the counter is free to count either up or down. The clock signal is transmitted from A19J1 pin 5 to the counter clock input A19I1 pin 15. The up/down line A19J1 pin 6 is inverted by A19I7C, and connected to the counter up/down input A19I1 pin 10. The counter is permanently wired for the binary count mode (A19I1 pin 9 is high (1)).

In the event that the counter A19I1 gets into an invalid code state (1010, 1011, 1100, 1101 or 1110) in the auto range mode, a feedback circuit automatically detects the invalid state and resets the counter to the 0110 state. A19I3A decodes the 1111 state. A19I7A decodes the 1001 and 1000 states. A19I2C decodes the 0111, 0110, 0101, 0100, 0011, 0010, 0001 and 0000 states. The outputs of these three decoders are NORed together by A19I7B. The output of A19I7B is high (1) during invalid states and low (0) during valid states. This output connects to switch A19I4B, which transmits the signal to the glitch swallower circuit A19I6 only in the auto range mode.

The glitch swallower circuit removes counter switching glitches caused by A19I1 non-synchronous counter outputs and differences in propagation delays for the three decoder circuits. Temporary invalid codes appear during these counter transitions that can last up to two CMOS propagation delay periods, causing glitches to appear on the error signal line going to the glitch swallower circuit. The glitch swallower circuit removes glitches with "on" times up to three CMOS propagation delays in length. The output of the glitch swallower A19I6C pin 10 is fed to the counter preset enable A19I1 pin 1. Any invalid code lasting more than three CMOS propagation delays will force the preset enable line high (1), causing the counter outputs Q0, Q1, Q2 and Q3 to preset to the jam input code of 0110. Normal level range changes, however, will not preset the counter.

4.3.2.2 Level Range Code Converter

The A19I1 counter output codes are converted to a code that is compatible with the operation of the dual input attenuator. The code lines are inverted by the A19I2 B, C, D and E inverters; this reverses the direction of the modulo counter (see table 4-4 for truth table). These inverted codes are connected to the "A" input port of a 4-bit full adder A19I9. This circuit adds a fixed binary number value of 1010 at the "B" input port to the inverted codes at the "A" input port. The A19I9 output code at port "S" is listed in the truth table in table 4-5; note that the carry out signal A19I9 pin 14 is not used. Output lines S3 and S4 of A19I9 are ORed together at A19I4D. The output of A19I4D is also shown in the truth table in table 4-5.

TABLE 4-4
AUTO RANGING UP/DOWN COUNTER.OUTPUT (INVERTED)

LEVEL RANGE ATTENUATOR POSITION	A19I2			
	PIN 6	PIN 12	PIN 10	PIN 4
−80 dBm	0	1	1	0
−70 dBm	0	1	1	1
−60 dBm	1	0	0	0
−50 dBm	1	0	0	1
−40 dBm	1	0	1	0
−30 dBm	1	0	1	1
−20 dBm	1	1	0	0
−10 dBm	1	1	0	1
0 dBm	1	1	1	0
+10 dBm	1	1	1	1
+20 dBm	0	0	0	0

TABLE 4-5
MODIFIED AUTO RANGING UP/DOWN COUNTER OUTPUT CODES

LEVEL RANGE ATTENUATOR POSITION	A19I9 PIN 13 S4	A19I4D PIN 11 S3+S4	A19I9 PIN 11 S2	A19I9 PIN 10 S1	A19I9 PIN 12 S3
−80 dBm	0	0	0	0	0
−70 dBm	0	0	0	1	0
−60 dBm	0	0	1	0	0
−50 dBm	0	0	1	1	0
−40 dBm	0	1	0	0	1
−30 dBm	0	1	0	1	1
−20 dBm	0	1	1	0	1
−10 dBm	0	1	1	1	1
0 dBm	1	1	0	0	0
+10 dBm	1	1	0	1	0
+20 dBm	1	1	1	0	0

4.3.2.3 Code State-of-Change Detector and Pulse Generator

This circuit detects changes in the level range code as well as 6040 power turn-on. It generates corresponding pulses to the dual input attenuator latching relays A3K1, A3K2, A3K3 and A3K4 to update the attenuator settings. The converted level range code coming from A19I9 (S1, S2, S4) and A19I4D pin 11 is connected to A19I10 (A0, A1, A2 and A3) and A19I11 (D0, D1, D2 and D3). The non-inverted latched outputs of A19I11 (Q0, Q1, Q2 and Q3) are connected to A19I10 (B0, B1, B2 and B3). A19I10 is a 4-bit magnitude comparator that compares the incoming converted level range code against previously stored codes in the quad latch A19I11. Refer to the timing diagram in figure 4-2 for a supplement to the remaining theory of operation. When the old and new codes are different, the comparator generates an error signal (A19I10 pin 3 goes low (0)), which is fed to the pulse generator circuit; this causes A19Q2 to begin discharging the timing capacitor A19C10, which intitializes the one-shot pulse sequence. After 181 micro-seconds, the timing capacitor voltage drops to 0.40 V DC, triggering comparator A19I12D, which sends a high (1) clock signal to the quad latch A19I11 pin 5. Latch inputs D0, D1, D2 and D3 now freely toggle to the latch outputs Q0, Q1, Q2 and Q3. The old and new codes at the 4-bit magnitude comparator inputs of A19I10 now match. This removes the error signal going to the pulse generator circuit and starts the one-shot pulse sequence. The constant current source (A19Q3 and associated resistors) starts charging the previously discharged timing capacitor A19C10. This capacitor's voltage increases linearily with time. After 10.6 milli-seconds, the timing capacitor voltage reaches 0.40 V DC, causing comparator A19I12D to switch and send a low (0) clock pulse to the quad latch A19I11, latching the code presently at its output. When the timing capacitor voltage reaches 5.20 V DC (148 milli-seconds after the start of the pulse sequence), comparator A19I12B switches high (1), causing the collector of A19Q5 to go low (0) and the collector of A19Q4 to go high (12 V DC).

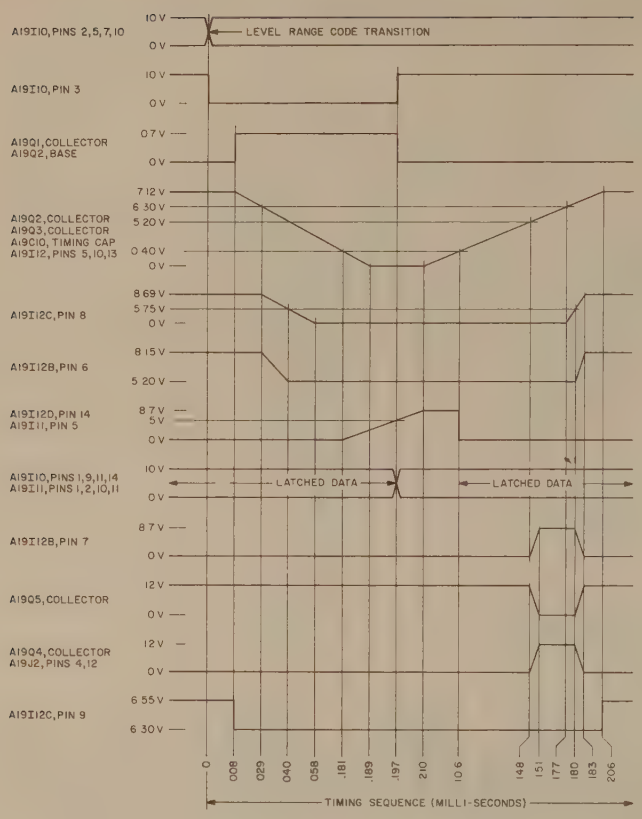


FIGURE 4-2
PULSE GENERATOR TIMING DIAGRAM

As a result of the collector of A19Q4 going high (12 V DC), the selected relay coils in the dual input attenuator are now energized. The timing capacitor voltage reaches 6.30 V DC, 32 milli-seconds later, causing comparator A19I12C to switch high (1), comparator A19I12B to switch low (0), the collector of A19Q5 to switch high (12 V DC) and the collector of A19Q4 to switch low (0). The selected relay coils in the dual input attenuator are now turned off. After a total elapsed time of 206 milli-seconds, the collector of A19Q3 reaches saturation, causing the timing capacitor to reach its maximum voltage level of 7.12 V DC, thus completing the one-shot pulse generation cycle. Note that when the 6040 is turned on, the timing capacitor is initially discharged causing the one-shot pulse sequence to be generated. This ensures that the dual input attenuator is initially at the correct level range setting. When the LEVEL dBm (MAX LEVEL) switch is turned quickly (less than 138 milli-seconds between detents), the pulse generator circuit will keep resetting the one-shot pulse cycle and will not generate any pulses to the dual input attenuator relays. When the final switch position is reached, the relays will then be switched to the final attenuator setting. A reduction in the number of times the relays have to switch and latch, improves the overall reliability of the 6040.

Latching relays are used in the dual input attenuator circuit to help conserve battery power drain. Each latching relay has two coils; one coil sets the relay and the other resets it. For each selected RANGE dBm (MAX LEVEL) position, one of the two coils will be selected on each relay and activated when the 32 milli-second pulse is generated by the auto ranging circuit. The quad latch A19I11 has 8 output lines (Q0, $\bar{Q}$0, Q1, $\bar{Q}$1, Q2, $\bar{Q}$2, Q3 and $\bar{Q}$3); they are the regular four converted level range codes plus the same four codes inverted. The 8 output lines of A19I11 drive 8 darlington transistors A19Q6 through A19Q13 which in turn selectively ground 4 of the relay coils. The 12 V, 32 milli-second output pulse connects to the other side of all 8 relay coils energizing only those four relay coils that are grounded.

CHAPTER 5
THEORY OF OPERATION FOR LOWPASS FILTER AND I.F.

5.0 GENERAL

The lowpass filter and I.F. circuitry are located on the A4 circuit board. Refer to figure 12-2 for the schematic diagram of the A4 board. A block diagram of the A4 board is shown in figure 5-1.

5.2 I.F.

The intermediate frequency circuit block consists of a dual conversion superheterodyne receiver with a final output frequency of 455 kHz. It contains the four following basic circuit blocks:

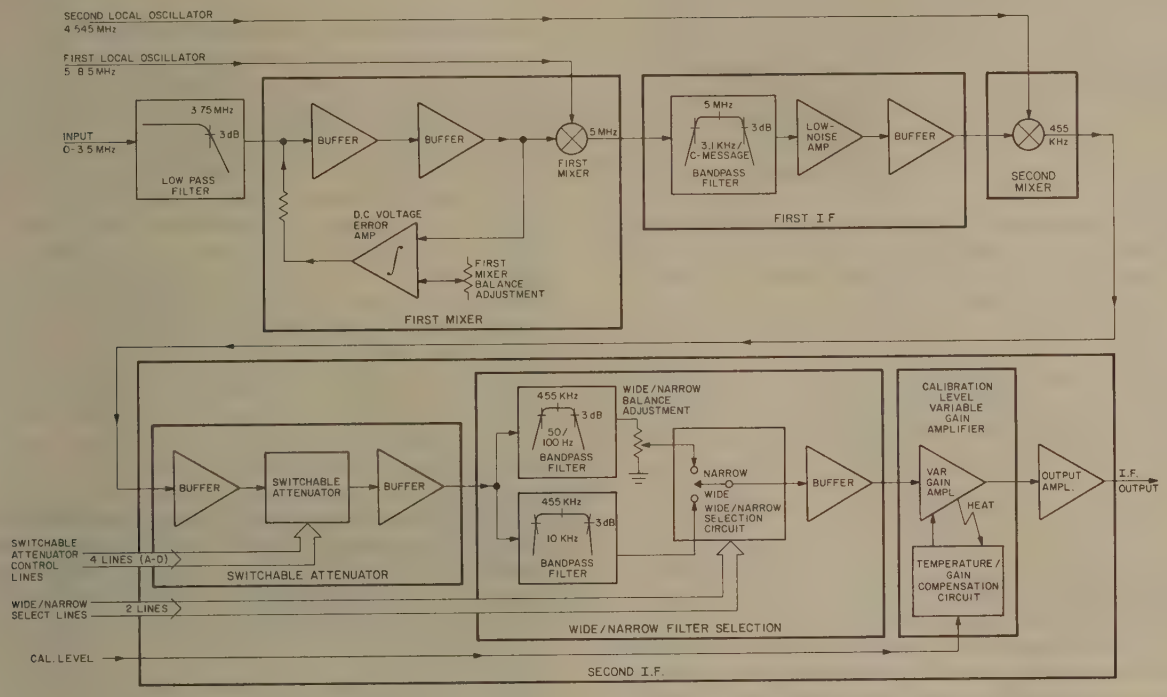


FIGURE 5-1 A4 PRINTED CIRCUIT BOARD BLOCK DIAGRAM

5.1 LOWPASS FILTER

The lowpass filter performs the following functions:

(a) It will pass all frequencies between 0 and 3.25 MHz with no rolloff or passband ripple.

(b) It begins to rolloff frequencies above 3.25 MHz (typically 0.25 dB at 3.5 MHz).

(c) For increases in frequency above 3.5 MHz, the amount of attenuation sharply increases until a minimum of 70 dB is reached at 5 MHz (it is necessary to have high attenuation at the first intermediate frequency (5 MHz) so that input signals at that frequency will not be coupled to the I.F.).

(d) A minimum of 70 dB attenuation is maintained at all frequencies above 5 MHz (the image frequencies lie in the frequency band between 10.0 and 13.5 MHz, and must be rejected by the lowpass filter).

The lowpass filter design is a Cauer Elliptic type. The input and output impedances are scaled to 120 ohms. The 3 dB bandwidth is set at 3.75 MHz. The stop band is designed for 74 dB attenuation at 4.7 MHz. The lowpass filter is composed of inductors A4L1 through A4L4, capacitors A4C1 through A4C9, and load resistor A4R2. Due to the use of low Q inductors, there is a 0.7 dB additional rolloff at 3.5 MHz. A passband equalizer circuit (A4R1, A4L5 and A4C10) is connected to the output side of the lowpass filter to compensate for the low Q inductors and to reduce the final rolloff at 3.5 MHz to 0.25 dB nominal.

(a) First Mixer
(b) First I.F.
(c) Second Mixer
(d) Second I.F.

5.2.1 First Mixer

The first mixer circuit block consists of two cascaded buffer amplifiers followed by the mixer.

The output of the lowpass filter is connected to the base of A4Q1c, a low-noise AC coupled emitter follower amplifier. This amplifier significantly lowers the 120 ohm input impedance, and provides the power gain necessary to drive the next amplifier stage. The emitter output of A4Q1c is connected to an active current source made up of A4Q1b and its associated circuitry; this greatly improves the dynamic range and low-distortion qualities of the amplifier.

The output of A4Q1c is connected to the bases of A4Q1a and A4Q2, which form a class-A complimentary symmetry amplifier. This circuit has matched sinking/sourcing capabilities, 50 ohm output impedance and DC coupling to properly drive the double balanced mixer circuit which follows. The output DC voltage is held constant by a feedback loop which integrates the output voltage (A4I1, A4R20 and A4C17) and compares it to the reference voltage (variable resistor A4R15). A DC error voltage is generated at pin 6 of A4I1 and is applied to the base of A4Q1c via a lowpass filter (A4R19 and A4C15).

The first mixer is a quad monolithic Schottky barrier diode ring (A4CR1) double balanced mixer. The DC coupled output of the complementary symmetry amplifier (A4Q1a and A4Q2) is connected to the mixer at the center tap of the mixer output transformer (A4T1). A frequency compensation circuit (A4R10 and A4C68) is connected between this line and ground to flatten the frequency response of the mixer between 12 kHz and 200 kHz. The first local oscillator signal (A4J2) is coupled to the mixer through a balun transformer (A4T2). A DC bias is applied to the mixer via the balun transformer. Good mixer balance is accomplished by using a matched monolithic diode ring (A4CR1), bifilar wound transformers (A4T1 and A4T2), and by adjustment of the DC voltage balance (A4R15). The mixer output (A4T1 and A4C21) is tuned to 5 MHz.

5.2.2 First I.F.

The first intermediate frequency block consists of a bandpass filter and two cascaded amplifiers.

The output of the first mixer (A4T1 and A4C21) is impedance matched to the WIDE bandpass filter A4FL1 (3.1 kHz or C-Message). The input of the low-noise MOSFET amplifier (A4Q3) is terminated (A4R17) to match the output impedance of the WIDE bandpass filter; the noise figure of the I.F. is set by this amplifier. The output of the MOSFET amplifier (A4T4 and A4C28) is tuned to 5 MHz. This output is fed to the base of A4Q6, an emitter follower amplifier which drives the second mixer input.

5.2.3 Second Mixer

The second mixer is a quad monolithic Schottky barrier diode ring (A4CR2) double balanced mixer. The AC coupled output from the emitter follower amplifier (A4Q6) is connected to the mixer at the center tap of the mixer output transformer (A4T5). The second local oscillator signal (A4J3) is coupled to the mixer through a balun transformer (A4T3). The mixer is operated at a DC ground voltage potential. There are no mixer balance adjustments. The mixer output (A4T5 and A4C34) is tuned to 455 kHz.

5.2.4 Second I.F.

The second intermediate frequency block consists of four minor sub-blocks:

(a) Switchable Attenuator
(b) WIDE/NARROW Filter Selection
(c) CAL LEVEL, Variable Gain Amplifier
(d) Output Amplifier

5.2.4.1 Switchable Attenuator

The purpose of the attenuator circuit is to make scaling corrections to the I.F. signal voltage levels associated with the different input impedances of the 6040. The unit will thus correctly display the selected input level in power (dBm). The output of the second mixer is connected to the base of A4Q4, an emitter follower amplifier. This amplifier drives a 4 ohm AC coupled load consisting of 11 individual voltage divider circuits, each with 41 ohm output impedances. The 11 voltage divider outputs are individually connected to a CMOS 16:1 analog multiplexer I.C. (A4I5). This I.C. allows selection of 1 of 16 input ports and connects the selected port to the common output port; the four unused input ports are connected to ground. Four control lines (A through D) determine which input is selected. The control lines receive their switching data from the IMPEDANCE switch (A2S2C), corresponding to various input impedances, bridged or terminated, as well as the CAL position. The output port of this I.C. (A4I5 pin 1) is coupled to a high input impedance buffer amplifier (A4I6) for further amplification.

5.2.4.2 WIDE/NARROW Filter Selection

The 6040 selectivity is achieved by first passing the first intermediate frequency (5 MHz) through the WIDE passband filter A4FL1 (3.1 kHz or C-Message), and then coupling the second intermediate frequency (455 kHz) through a choice (front panel selectable) of a NARROW passband filter A4FL2 (50 or 100 Hz) or an extra WIDE passband filter A4FL3 (10 kHz). The narrow filter superimposes its own nose and skirt characteristics upon the signal. The extra wide filter does not affect the nose of the wide filter (A4FL1), but does add to the ultimate skirt attenuation of the system. Both filters (A4FL2 and A4FL3) are connected to the output of A4I6 (pin 6). The output of the extra wide filter is loaded with a fixed voltage divider (A4R83 and A4R84). The narrow filter output is loaded with an adjustable voltage divider (A4R83 and A4R84), that is adjusted (±3 dB range) to equalize the center passband voltage levels of the two selectable filters. The two voltage divider outputs are connected to a CMOS analog transmission gate switching arrangement (A4I7 and A4I8), controlled by digital signals from the front panel SELECTIVITY switch. Several switching stages are required to turn off the wide filter signal (A4I8a, A4I8b, A4I8d, A4I8c, A4I7c, A4I7b); the signal must be attenuated by a minimum of 80 dB, so that the narrow filter skirts will not be effectively raised by the wide filter passband feedthrough in the switching circuit. The switching circuit output is coupled to a high input inpedance amplifier (A4I9) for additional buffering and voltage gain.

5.2.4.3 CAL LEVEL, Variable Gain Amplifier

The output of A4I9 (pin 6) is coupled to the input of A4I10 (pin 4), an externally controllable variable gain amplifier. The CAL LEVEL potentiometer, located on the 6040 front panel, is rotated to adjust the I.F. gain (±6 dB nominally). A full mechanical rotation of 270 degrees gives a corresponding potentiometer linear output voltage range between 0 and 10 V DC. The CAL LEVEL output voltage is connected to the temperature compensation circuit, which consists of A4Q8 and associated components. A4Q8 performs two separate functions. First, it modifies the CAL LEVEL output voltage and couples it to the variable gain amplifier. Secondly, A4Q8 is mechanically secured to A4I10 and acts as a temperature sensor, automatically holding the overall 6040 gain nominally constant during intitial unit turn-on and warm-up periods, as well as during ambient temperature deviations.

5.2.4.4 Output Amplifier

The output of A4I10 is coupled to the base of A4Q5, an emitter follower amplifier. The emitter of A4Q5 is connected to an active current source consisting of A4Q7 and associated components; the current source allows A4Q5 to make large distortionless voltage swings. The output signal is capable of delivering a linear voltage swing of up to 8 V p-p into a 2,500 ohm load.

CHAPTER 6
THEORY OF OPERATION FOR FREQUENCY GENERATION, CONTROL AND DISPLAY

6.0 GENERAL

The circuitry pertaining to the frequency selective function of the unit is contained on circuit boards A7 through A12. A9 and A10 circuit boards comprise most of the 1st L.O. and the 1st L.O. buffer circuitry. The A12 circuit board contains the 2nd L.O. The A11 circuit board includes a TCXO used as a reference oscillator and two phase lock loops used to control the L.O. frequencies. The A8 circuit board contains circuitry to generate the time base and other control signals for the frequency counter. A8 also provides circuits used to generate frequency difference signals with the final difference signal acting as the count input to the frequency counter. The A7 circuit board contains the frequency counter with the LCD drivers and LCD display.

6.1 FREQUENCY GENERATION

The 1st L.O. circuit board A9, 1st L.O. Buffer circuit board A10 and tuning capacitor A16C1 are contained within the 1st L.O. assembly A16. The schematic diagram for this circuitry will be found in figure 12-3.

6.1.1 1st L.O. A9

The 1st L.O. has a frequency range of 5.0 to 8.5 MHz. The resulting input frequency band is divided into four overlapping ranges: 0.3-650 kHz, 550-1650 kHz, 1300-2400 kHz and 2000-3500 kHz. A9S1 is the RANGE kHz switch. The circuitry associated with A9Q1 forms a common collector Colpitts type oscillator. The resonant tank circuit inductor is A9L1. The capacitance portion of the resonant tank circuitry consists of an array of capacitors configured by the position of switch A9S1. Varactor diode A9CR2 and coupling capacitor A9C2 are connected in parallel with the tuning capacitor A16C1. In an AFC mode, the control voltage to A9CR2 applied at A9E4 will shift the 1st L.O. frequency in a direction such as to maintain a 455 kHz 2nd I.F. output frequency. When not employed in the AFC mode, the component of the A9E4 control voltage which is supplied by the FINE TUNE control may be used to fine tune the unit.

The emitter follower A9Q2 reduces the load placed on the oscillator and provides the current gain and isolation needed to drive the buffer circuitry.

6.1.2 1st L.O. Buffer

1st L.O. Buffer circuitry is located on circuit board A10. The buffer circuitry converts the oscillator output to a 50% duty cycle square wave signal for use by the I.F. It also provides a TTL compatible signal required by the frequency control and display circuitry.

Transistors A10Q1 and A10Q2 simply provide voltage gain. Differential amplifier A10Q3 and A10Q4 act as a comparator to generate a square wave signal. The comparator has been designed to guarantee a 50% duty cycle output for the full range of 1st L.O. frequencies. Transistors A10Q5 and A10Q6 are configured as a complementary emitter follower and provide the current gain needed to drive the I.F. 1st mixer injection input. Transistor A10Q7 provides a TTL compatible signal at its collector for a 1st L.O. input to the A8 board.

6.1.3 2nd L.O. A12

A12Q1 is a crystal controlled Colpitts oscillator with a nominal operating frequency of 4.545 MHz determined by crystal A12Y1 and the capacitance of A12CR1. The control voltage to the varactor A12CR1 is generated by a phase locked loop on board A11 which, in turn, maintains the 4.545 MHz 2nd L.O. frequency to the accuracy of the TCXO.

The output from A12Q1 is amplified and shaped by A12I2, Q2 and Q1 circuitry. NOR gate A12I2D acts as an AC coupled self-biasing inverter. The A12I2D inverter converts the oscillator output to logic levels. Gates A12I2C and A12I2A are connected in parallel in order to provide current drive capability. Gate A12I2B produces an output signal that drives the A8 2nd L.O. input. Transistors A12Q2 and A12Q3 form a complementary emitter follower with the low impedance output required to drive the 2nd I.F. mixer.

6.2 A8, A11 and A25 FREQUENCY CONTROL

The block diagram shown in figure 6-1, shows the various functions performed by digital circuits contained on the A8 and A11 circuit boards. Schematic diagrams of these boards plus A7 and A25 are shown in figure 12-4. Frequency signal inputs to these boards enter at A8E2, A8E4 and A8E6.

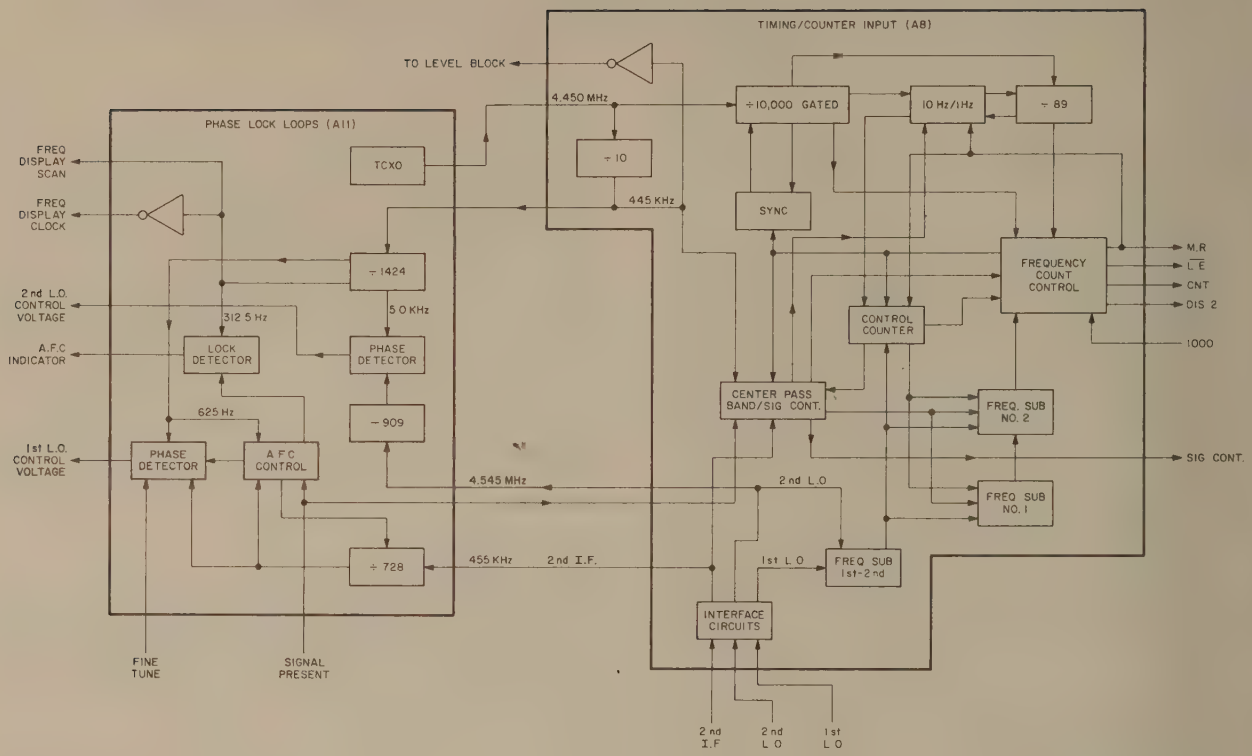


FIGURE 6-1 FREQUENCY CONTROL AND DISPLAY

Each signal travels through a portion of the interface circuitry block. The 2nd I.F. signal is sinusoidal and varies in amplitude. A comparator A8I19A is used to provide a 2nd I.F. signal at CMOS logic levels. The 1st L.O. signal drives the pin 4 input to XOR gate A8I20B. A8I20B supplies signal shaping and drives the 1st L.O. input to the frequency subtractor circuits.

NOR gate A8I21A converts the 2nd L.O. signal from an 8 V p-p to a 10 V p-p signal. The voltage divider consisting of A8R2 and A8R1 with emitter follower A8Q1 converts the CMOS 2nd L.O. signal to a TTL signal for driving A8I22A.

The heart of the frequency associated circuitry is the TCXO (A11MY1) located on the A11 board. The associated phase locked loop's (PLL's) used to control L.O. frequencies are also located on A11.

6.2.1 A11 2nd L.O. Phase Locked Loop

The TCXO 4.450 MHz output goes from A11 to A8. On board A8 the signal is divided by 10 in decade counter A8I24. The 445 kHz output from this counter is used on A8, A11 and also A21. On A11, BCD counters A11I1A and A11I1B, flip-flop A11I7A and NAND gate A11I2B divide the 445 kHz signal by 89 to a 5.0 kHz signal. This 5.0 kHz signal establishes a reference frequency input for the XOR gate A11I10B. The output of A11I10B is integrated by A11R5, A11R6 and A11C5 providing a phase detector output for the control of the 2nd L.O. frequency.

The 2nd L.O. signal from A8I21A is divided by a factor of 909 to drive the second input to the phase detector A11I10B. Four bit shift registers A11I8A and A11I8B along with flip-flop A11I3A form a divide-by-9 shift counter. This particular configuration was chosen to overcome propagation delay problems that might arise with more conventional circuits.

Decade counters A11I9A and A11I9B together with flip-flop A11I7B and XOR gate A11I10C form a divide-by-101 circuit. Normally, the pin 1 input to A11I9A is LO, enabling a count for each input from A11I8B. Each time the Q3 output of A11I9B goes HI, the resulting HI output from gate A11I10C inhibits the counting of A11I9A. With the next fall of the A11I8B-Q2 signal flip-flop A11I7B is set and the inhibit input to A11I9A is removed. With the fall of the A11I9B-Q3 signal flip-flop A11I7B is asynchronously cleared and no count inhibit signal is generated. By inhibiting one count per 100 counts of the primary counter a divide by 101 function is accomplished. The cascaded frequency dividers provide a divide-by-909 function and provide for a 4.545 MHz 2nd L.O. frequency under phase lock conditions.

6.2.2 A11 AFC Phase Locked Loop

For the AFC loop, the 5.0 kHz from A11I1A-Q4 is divided by 8 by binary counter A11I5A to give a 625 Hz reference frequency. The 312 Hz signal derived from A11I5A-Q4 is used to clock the lock detection counter and LCD display.

The 2nd I.F. signal is divided by 728 in two steps. In the first step the divide by 91 divider consists of decade counters A11I4A and A11I4B together with NAND gates A11I2A and A11I2C. The second step divide-by-8 function is performed by binary counter A11I5B.

The AFC phase detector consists of XOR gates A11I10A and A11I10D. The reference input to A11I10A pin 1 comes from A11I5A-Q3 while the divided 2nd I.F. signal from A11I5B-Q3 provides the A11I10A pin 2 input. When operating in an AFC active mode, the pin 12 input to XOR gate A11I10D is LO while the second gate input comes from the output of gate A. The LO control input to A11I10D means that gate D output will follow

the gate A output. The gate signals add to control the integrated phase detected signal on A11C2.

When the unit is not in an active AFC mode, a HI input to A11I10D pin 12 will cause the D gate output to be the inverse of the A gate output. The combined outputs of the gates cancel, yielding a constant +5.0 V contribution to the A11C2 voltage by the two gates. The A11C2 1st L.O. control voltage can now be controlled only by the voltage contributed by the FINE TUNE control.

The AFC control block consists of flip-flops A11I3B, A11I6A and A11I6B. The control block is in a ready state when A11I3B and A11I6A are cleared and A11I6B is set. In the ready state, the HI input to A11I10D pin 12 inhibits phase detection and the HI input to A11I4B pin 9 holds the 2nd I.F. divider at a ready count. The input signal at A11E1 is provided by the AFC switch and a signal validity output from the A21 board. The signal will be HI when the switch is in the AFC position and the selected input signal has a level above the threshold of the level display circuitry. The A11E1 signal is sampled by A11I5A-Q3 and A11I6A is set by the rise of A11I5A-Q3 when the A11E1 signal is HI. The setting of A11I6A sets A11I3B. A set A11I3B enables the 2nd I.F. divider. The LO signal from A11I6A-$\bar{Q}$ provides a LO input to A11I10D activating the phase detector and also removes the reset input from the binary counter A8I18. The ready count for the 2nd L.O. divider and the A11I6A clock signal have been selected so that the loop is activated with the frequency dividers in a locked phase relationship. Flip-flop A11I6B monitors the phase relationship between the two phase detector signals. As long as the loop remains in a locked state, A11I6B will remain set. A11I6A and A11I3B will also remain set provided the signal at A11E1 remains HI.

In the event that the control voltage to the 1st L.O. does not maintain a 455 kHz 2nd I.F. frequency the disintegrating phase relationship between the phase detector inputs will clear A11I6B. With A11I6B cleared, a HI input to the reset input of A11I6A also clears A11I6A. With both A11I6A and A11I6B cleared the AFC control block is now in an unlocked state and the lock detector counter is reset. During a locked state A11I3B is held set by a HI set input. In the unlocked state A11I3B will remain set until the 2nd I.F. inputs to the 2nd L.O. divider advance it to a ready count. The ready count is sensed when the Q2 output of A11I5B goes HI while the Q3 output is LO. This condition clears A11I3B. The clearing of A11I3B in turn provides a HI set input to A11I6B. The clearing of A11I3B and the setting of A11I6B return the blocks to a ready state with the 2nd L.O. divider held in the ready count state.

If, after the loop is placed in a locked condition, control of the 1st L.O. frequency maintains a locked condition, the A8I18 lock detector counter will be advanced to a 128 count. For a 128 count A8I18B-Q4 will be HI and further counting will be inhibited. The HI at A8I18B-Q4 is also connected to the A7 input which generates an AFC indication in the LCD frequency display margin.

6.2.3 A25 Low Pass Filter

The A25 board contains an active, line shunting low pass filter. This filter removes the 1.25 kHz frequency component from the 1st L.O. control signal.

6.3 A8 COUNT SIGNAL GENERATION

The majority of the circuitry on the A8 board can be divided into two major blocks. One block generates the count signal input for the frequency display, while the second block generates the counter time base with reset and latching signals. The lower half of the schematic for A8 shown in figure 12-4 shows count signal generation circuitry.

The frequency display counter has a count interval of 0.2 seconds. In order to obtain a 10 Hz resolution display, a signal at half the frequency to be displayed must be counted.

$$\text{Counts} = f_o/2 \text{ Hz} \times 0.2 \text{ sec.} = 0.1\ f_o \text{ counts}$$

When in a signal count mode the count signal $f_o/2$ generated is $f_{in}/2$. For the center passband mode of operation, the count signal generated is $(f_{in}/2 + 5000)$. In the center passband mode the additional 1,000 counts are subtracted from the display by inhibiting the counting of the 4th digit until after count 1,000.

The 6040 heterodyning scheme uses the following frequency relationships:

$$\text{Equation 1: f 1st I.F.} = \text{f 1st L.O.} - f_{in}$$
$$\text{Equation 2: f 2nd I.F.} = \text{f 1st I.F.} - \text{f 2nd L.O.}$$

Rearranging equation 2 gives:

$$\text{f 1st I.F.} = \text{f 2nd I.F.} + \text{f 2nd L.O.}$$

By substitution, equation 1 becomes:

$$\text{f 2nd I.F.} + \text{f 2nd L.O.} = \text{f 1st L.O.} - f_{in}$$

Rearranging the above equation gives:

$$f_{in} = (\text{f 1st L.O.} - \text{f 2nd L.O.}) - \text{f 2nd I.F.}$$

Finally, dividing by 2 gives:

$$f_{in}/2 = (\text{f 1st L.O.} - \text{f 2nd L.O.})/2 - (\text{f 2nd I.F.})/2$$

When a signal is being detected, the 2nd I.F. output can be used to generate a signal count display. When a center passband display is desired or required the 445 kHz signal, 10 kHz below the 455 kHz 2nd I.F. frequency, is used to generate the count signal. This will generate the $(f_{in}/2 + 5000)$ frequency previously discussed.

6.3.1 1st L.O. 2nd L.O. Frequency Subtractor

The L.O. difference frequency circuits used to generate the (1st L.O. − 2nd L.O.)/2 signal are A8I22A, A8I23 and A8I20C. Gate A8I21B converts the TTL L.O. difference signal to CMOS logic levels.

The L.O. difference has a frequency equal to (f 1st L.O. − f 2nd L.O.)/2. This signal first appears at the output of the XOR gate A8I20C. The pin 10 input to this gate is derived from A8I23 flip-flop "D" and will be a square wave having a 1st L.O./2 frequency. Flip-flop "D" is configured to toggle with the 1st L.O. clock input to the register. The 2nd A8I20C input is derived from A8I23 flip-flop "A". The D input to flip-flop "A" is provided by flip-flop A8I22A which is toggled by the 2nd L.O. and has a 2nd L.O./2 output frequency.

The A8I23 "A" flip-flop will change state at a 2nd L.O./2 rate, but these changes of state are synchronized with the 1st L.O. clock input to the register. The output of gate A8I20C will change state anytime the 1st L.O./2 signals changes state without a change to the 2nd L.O./2 signal. Whenever both inputs to the gate change state, the gate output will remain unchanged. This means that the output of the XOR gate A8I20C will change states at a (1st L.O.) − (2nd L.O.) rate and will have a (1st L.O. − 2nd L.O.)/2 average output frequency. Any unwanted switching transitions generated at the output of A8I20C are removed by the sampling action of A8I23 flip-flop "B".

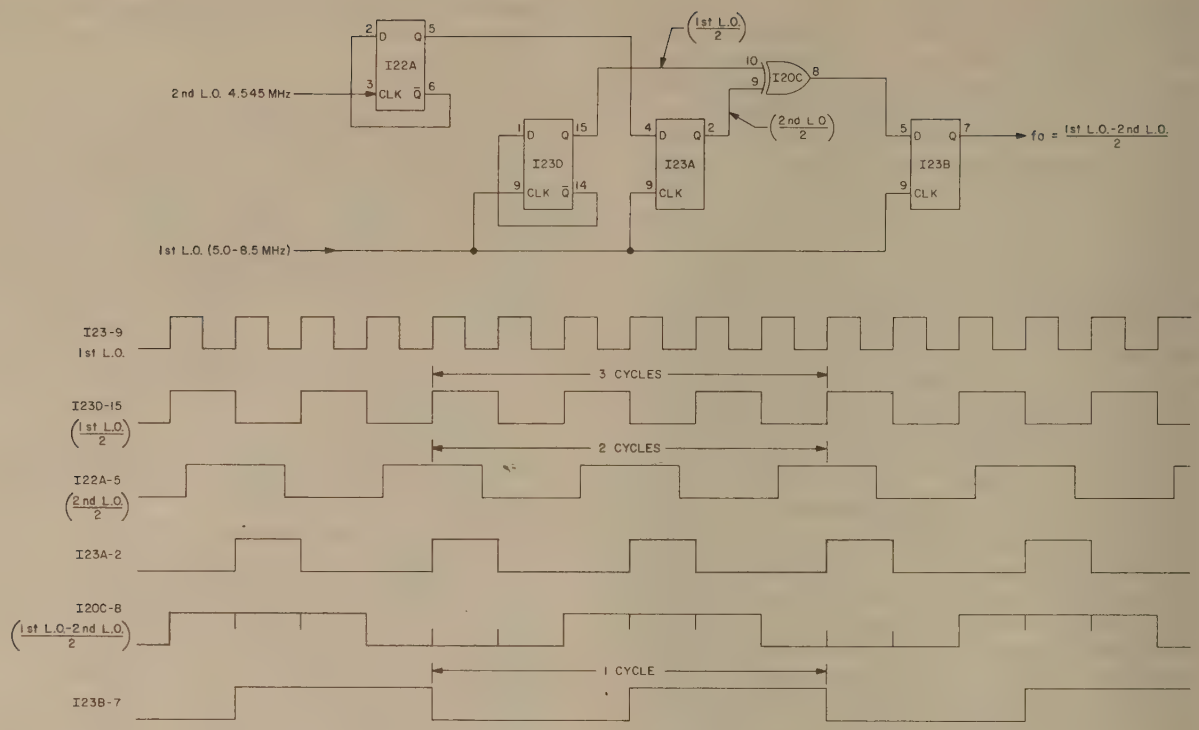


FIGURE 6-2 1st L.O. − 2nd L.O. FREQUENCY SUBTRACTOR

6.3.2 Control Counter

The control counter is used to make two decisions regarding the frequency display system. The first decision is the selection of one of two subtractors involved in producing a frequency counter input. Two different subtractors are required to subtract the 2nd I.F. signal from the L.O. difference signal. Subtractor #1 will operate down to a zero frequency difference, but will not work for large differences in frequency. The #2 subtractor does work for large frequency differences but generates errors at frequency differences near zero. The frequencies at which the two subtractors have overlapping frequency ranges is within the 0.3 to 650 kHz frequency band and the switching between subtractors cannot be accomplished by the RANGE kHz switch. Any time the L.O. difference signal used to clock the control counter, advances the counter to the max count, subtractor #2 will be active.

The second decision determines the forcing of the frequency display to all "zero's". When the L.O. difference signal frequency falls below the frequency required for a minimum control count, an all "zero" frequency display is forced, thus informing the operator that he has tuned the unit below the unit frequency range.

The control counter block consists of A8I13, A8I14, A8I12A and A8I15. A8I13 is a decade counter with decoded outputs, A8I14 is a 14 stage ripple counter and A8I12A is a BCD counter. Flip-flop's A8I15A and A8I15B are clocked at the end of each frequency count and sample the condition of the control counter. A HI at the D input of A8I15A means that the counter has reached its maximum count. Clocking the flip-flop with the HI D input will set the flip-flop and the HI Q output will activate subtractor #2 holding off subtractor #1.

Flip-flop A8I15B samples the Q13 output of A8I14. If A8I14-Q13 does not reach a HI state during the control counter count interval, the unit is tuned below the unit frequency range. A "LO" sampled at the D input to A8I15B will provide a HI output at A8I15B-$\bar{Q}$. A HI input to gate A8I8C pin 13 from A8I15B generates a frequency count master reset signal with a premature rise time which resets the count to be displayed prior to latching.

The count interval for the control counter is controlled by the reset input to A8I13. Flip-flop A8I16B is set at the start of each frequency count interval and the control counter is enabled. A8I16B remains set for about 18 milliseconds. The HI on the A8I13 reset input inhibits counting while A8I14 and A8I12A remain at the count obtained until after A8I15 flip-flops have been clocked at the time of a frequency count LATCH ENABLE (L.E.) signal. The display count MASTER RESET (M.R.) signal is used to reset A8I14 and A8I12A. Feedback from A8I12A output Q3 to the A8I13C CE input inhibits further counting after the maximum count has been reached. While counting, the A8I12A stages remain at zero until after A8I14-Q13 reaches its HI state.

6.3.3 Subtractor #1

Subtractor #1 consists of A8I25, A8I27D and A8I26. A8I25B and A8I26B are common to both subtractors. A8I26B is connected to toggle with each clock input. The A8I26B output will have a frequency of 222.5 kHz or the 2nd I.F./2 depending on the inputs from flip-flop A8I16A to the AND-OR-INVERT gates of A8I25B.

Subtractor #1 works on a phase shift detection principle. The ouput of A8I25A will be positive pulses having about a 25% duty cycle. When the A8I25A output is HI, XOR gate A8I27D feeds

back the inverted Q output of A8I26A to the D input. This means that the clocking of A8I26A while the A8I25A output is HI will toggle A8I26A.

Each time flip-flop A8I26A toggles, the inputs to A8I25A at pins 1 and 13 reverse and output of gates A8I25A shift 180° in phase. It follows that A8I26A will toggle again after a 180° phase shift occurs between the 2nd I.F. generated signal at the D input of A8I26A and the L.O. difference signal at the A8I26A clock input. The fact that the flip-flop toggles each time there is a 180° shift in phase between the two signals means that the flip-flop will have an output frequency equal to the difference between the two frequencies or, in this particular case, the output frequency will be:

$$(f\ 1st\ L.O. - f\ 2nd\ L.O.)/2 - f\ 2nd\ I.F./2$$

For the signal count mode of operation this difference frequency will equal one-half the input frequency.

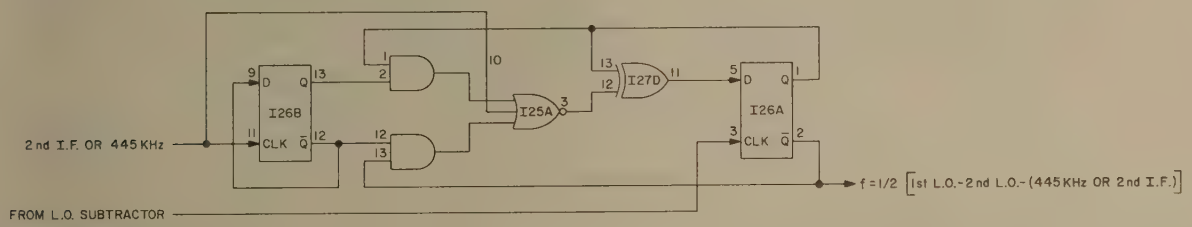
For a center pass band mode of operation the 445 kHz input to gates A8I25B is substituted for the 2nd I.F. input. This will generate a subtractor output frequency 5.0 kHz high. The higher frequency signal is compensated for by subtracting 1000 counts in the signal counting process.

Subtractor #1 is held off by a HI set input to A8I26A at pin 6. The two subtractor output signals are gated together by gate A8I27C.

6.3.4 Subtractor #2

Subtractor #2 comprises shift register A8I28 and XOR gates A8I27A and A8I27B. This frequency subtractor operates in an identical manner to that of the 1st L.O. 2nd L.O. subtractor. The clock signal required for the register must be equal to the change rate of the highest of the two frequencies in the formula (fa — fb)/2. The output of XOR gate A8I27B will generate the required clock signal. Each time the A8I27B input to pin 5 changes state, the HI going signal clocks A8I28A. The toggling of A8I28A changes the input to pin 6 of A8I27B and removes the HI signal that clocked the register. This removal of the HI generated by the pin 5 change means the next change will also generate a HI pulse and HI pulses will be generated at the pin 5 input change rate.

The pin 2 input to XOR gate A8I27A will be the L.O. difference signal, while the pin 1 input will be the 2nd I.F./2 signal derived from flip-flop A8I26B, and synchronized by the clock input to A8I28D. The output of A8I27A will have an output change rate equal to L.O. difference minus the 2nd I.F. change rate. Since two changes constitute a cycle, the output frequency will be (L.O. difference — 2nd I.F.)/2. This frequency difference signal will provide the 2nd input to A8I27C. The output of A8I27C is used to clock the frequency display counter. A LO on A8I28 pin 1 will hold off subtractor #2 while subtractor #1 is allowed to operate.



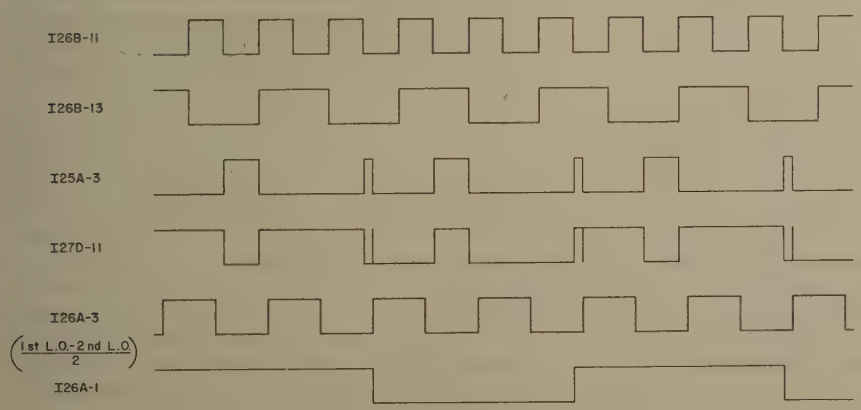


FIGURE 6-3
SUBTRACTOR #1

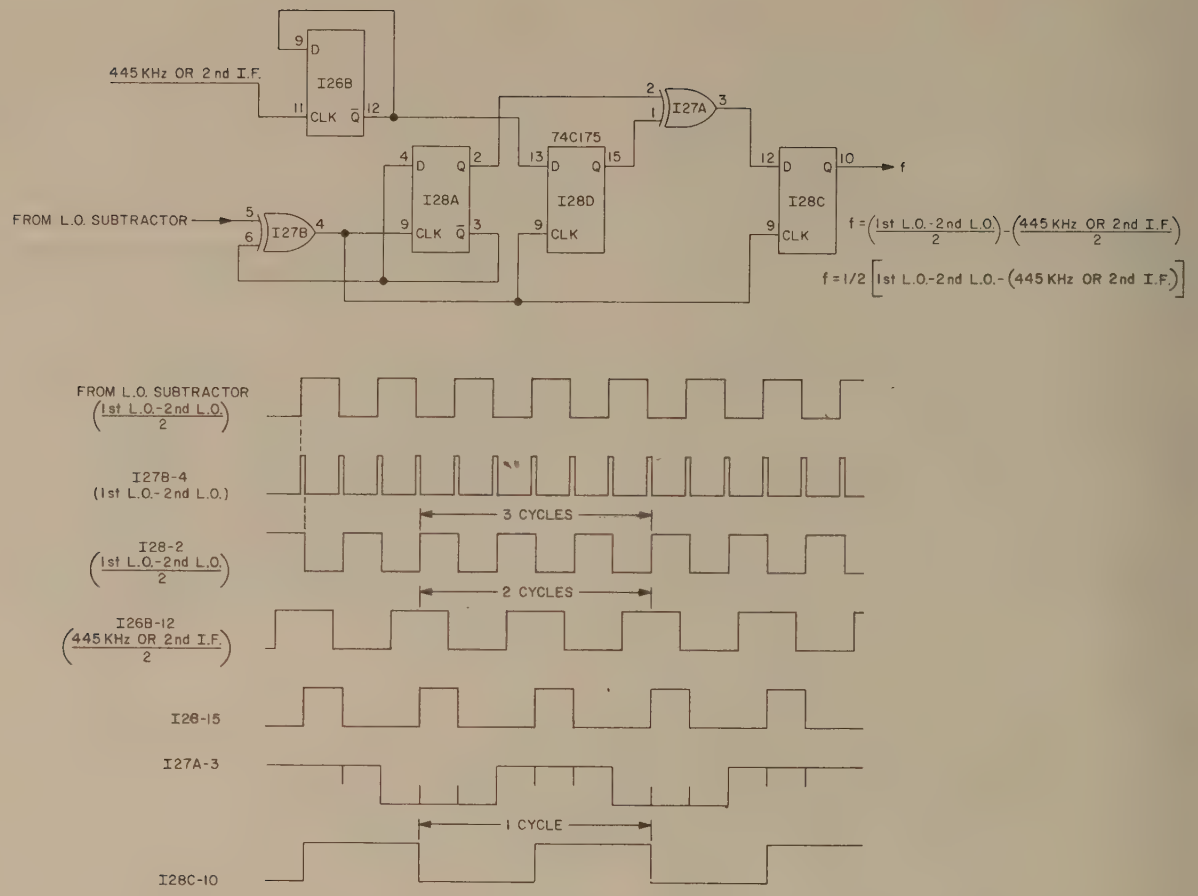


FIGURE 6-4
SUBTRACTOR #2

6.4 FREQUENCY COUNT AND DISPLAY

The frequency counter and LCD frequency display are contained on board A7. Board A8 contains the circuitry required to generate the counter time base, along with the latching, resetting and other signals necessary to display a frequency count. A8 blocks pertaining to the frequency display are shown in figure 6-1. A7 and A8 schematic diagrams are shown in figure 12-4.

6.4.1 10,000 Divider

The 10,000 Divider block consists of four decade counters A8I1, A8I2, A8I3A and A8I3B. These counters make up the first four stages of the frequency divider used to generate the frequency display time base from the 4.45 MHz TCXO output.

The first divider stage, A8I1, has a reset input provided by the SYNC block at the end of each count interval and after LATCH ENABLE and MASTER RESET pulses have been generated, a HI reset input to A8I1 holds A8I1 in a zero count state. The reset input is removed on the rising edge of the frequency display count signal. This means count errors can approach ±½ L.S.D. and least significant digit jitter is held to a minimum.

In addition to generating a frequency division of ten, A8I2 also provides decoded outputs that are used to generate the latching, resetting and other clocking pulses required for the frequency counter initializing process. A low output from A8I10B will hold A8I2 at the count 4 state after the frequency counter has been initialized. A8I2 will be reset and enabled by the action of the SYNC block as a new frequency count is started. BCD counters A8I3A and A8I3B only provide divide by ten functions.

6.4.2 10 Hz/1 Hz

The 10 Hz/1 Hz block consist of BCD counter A8I12B, AND-OR-INVERT gates A8I4A and A8I4B, flip-flops A8I11A, A8I11B, A8I16B and NAND gate A8I10D.

The AND gates of A8I4 have inputs from A8I11B that control which signal will clock A8I5B and which signal will generate a LO input at A8I16B. Normally, A8I11B will be in a set state which provides a 10 Hz resolution operation. Counter A8I5B will be advanced by counter A8I3B and the resetting of A8I16B will be enabled by A8I5A. A8E17 will be grounded by the DISPLAY switch when in the 1 Hz position. If a valid input signal is being detected, A8I16A of the center pass band/signal count blocks will be reset. A reset A8I16A permits the resetting of A8I11B. A8I11B is clocked by the MASTER RESET signal. When reset, A8I11B extends the frequency count interval to 2 seconds by gating the output A8I12B to the input of A8I5B. This adds one more decade to the count interval divider. A reset A8I11B also maintains the control counter count interval to 18 milliseconds by gating the A8I5B output Q4 to the D input of A8I16B. Once A8I16 is reset, feedback to pin 10 of A8I4A maintains a low D input unti' the next count interval.

A8I11A controls the decimal point displayed. A8I11A is reset one MASTER RESET pulse later than A8I11B following the completion of a 2 second frequency count. NAND gate A8I10D provides a low input to A8I11B input D during the first 2 second count interval. This means that once A8I11B has been reset a 1 Hz

resolution frequency display will be seen for a minimum of 2 seconds provided that the signal remains at a detectable level.

6.4.3 89 Divider

The 89 divider consist of A8I5A, A8I5B, A8I6C and A8I7A. A8I5A and A8I5B are BCD counters and NAND gate A8I6C decodes the count 89 state of the A8I5 counters. Flip-flop A8I7A is used to sample the output of A8I6C and synchronizes the end of a count interval with the rise of the carry output of A8I2. This action eliminates the propagation delays through the A8I3 and A8I5 counters and other gates from having any effect on the count interval.

6.4.4 Frequency Count Control

The Frequency Count Control blocks consist of gates A8I8A, A8I8C, A8I8D, A8I6B, A8I10A and flip-flop A8I7B. These circuits control the gating of the count signal to the counter and the generation of latching and resetting signals.

During a frequency count interval, flip-flop A8I7A of the divide by 89 block, will be set and A8I7A will provide a low input to NAND gate A8I10A. With a HI output from A8I10A providing a HI set input to A8I7B, the $\bar{Q}$ output from A8I7B will follow the count signal at the reset input. When the set input to A8I7B goes LO any LO output from $\bar{Q}$ will remain LO until the reset input goes HI. This means that an abnormally short negative pulse cannot occur at the end of a count interval. The input to A8I10A from A8I9B prevents any delay in the start of a count interval resulting from propagation delays through A8I5, A8I6C and A8I7A.

At the end of a frequency count interval, the resetting of A8I7A will inhibit any further count pulses and will provide a LO enable input to NOR gates A8I8A and A8I8C. Provided that the $\bar{Q}$ output of flip-flop A8I17B is HI, the HI from A8I8A will result in a LO going latch enable output from NAND gate A8I6B on count 1 of A8I2. On the 3 count of A8I2, NOR gate A8I8C will receive a LO input from A8I8D and a HI MASTER RESET pulse will be generated. When the unit is tuned too low, a HI from A8I15B to A8I8D will generate an early rise of the MASTER RESET pulse and cause all "zero's" to be latched and displayed.

The rise of the A8I8A output at the end of a frequency count interval is used by both the SYNC and pass band/signal count blocks for sampling or gating.

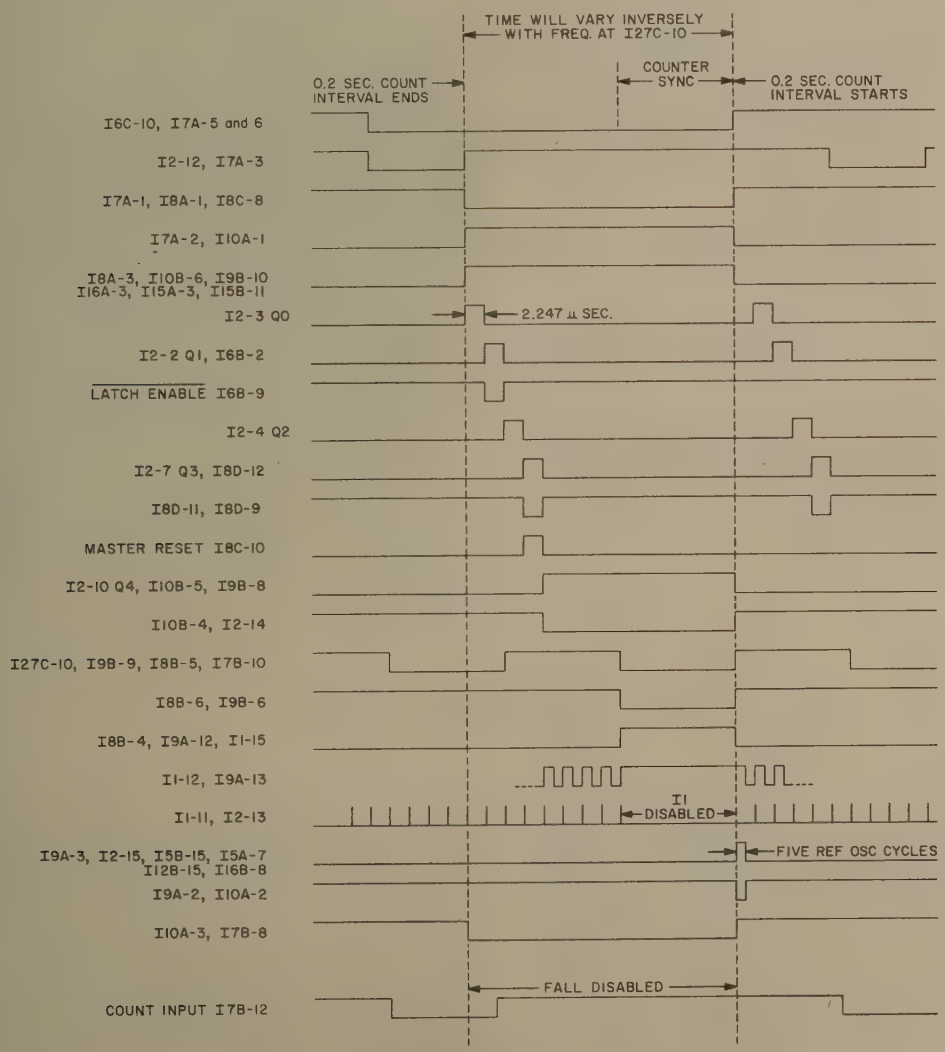


FIGURE 6-5
A8 FREQUENCY COUNT CONTROL SIGNALS

6.4.5 SYNC

The SYNC block consist of flip-flops A8I9B and A8I9A and gates A8I10B and A8I8B. A8R14 and A8C5 also belong to this block.

During a frequency count interval, both A8I9 flip-flops will be in a reset state. The count interval will end on a zero count of A8I2. The HI output from A8I8A will enable A8I10B. On count 4 of A8I2 a LO output from A8I10B will inhibit any further counting of A8I2. The HI inputs to A8I9A at R and J means A8I9A will be set on the fall of the count signal. With a LO count signal and a set A8I9A, NOR gate A8I8B will hold counter A8I1 in a reset state. When the A8I8B output falls with the rise of the count signal a new frequency count interval will be intitiated. The fall of the A8I8B output will set flip-flop A8I9B, which in turn resets counters A8I2 and A8I5A. A8I5B sets flip-flop A8I7A and provides a LO input to A8I10A. This enables A8I7B to gate through count pulses. A8I9B will be reset when A8I1 reaches a 5 count. A8I9A will be reset when A8I8A returns to the LO state as a result of A8I5A and A8I5B being reset.

A special condition arises when the unit is tuned near "zero" frequency and this "zero" frequency lies within the passband. In this case the count signal frequency will go to "zero" and the display will remain unchanged. If flip-flop A8I7A remains reset for about 0.1 second, capacitor A8C5 will be charged to a voltage which will provide a HI input to A8I8A. The HI input to A8I8A will result in the setting of A8I9A and a HI output from A8I10B. This action starts a new frequency count interval in the absence of a count signal rise.

6.4.6 Center Pass Band/Signal Count

The center pass band/signal count block comprises flip-flops A8I16A, A8I17A and A8I17B, gates A8I10C and A8I6A and AND-OR-INVERT gate A8I25B.

A LO output from A8I10C will enable A8I6A to be clocked to a reset (SIGNAL COUNT) state at the end of a frequency count interval.

When A8I16A is reset, the HI reset input to A8I17A will hold A8I17A reset. Simultaneously, the disenable input to the 2nd three stages of the frequency counter of A7 will remain enabled for a complete count interval. Inputs to A8I25B will gate the 2nd I.F. signal to A8I26B.

The output of A8I10C will go HI setting A8I16A to a CENTER PASS BAND state any time A8E11 is brought LO by the A21 board in the absence of a detected signal or alternatively, A8E12 is grounded by the DISPLAY switch in its CENTER PASS BAND position or again, when A8I15B is reset as a result of too low a tuned frequency.

When A8I16A is set, A8I17B will be clocked to a reset state. With A8I17B reset, a LO input to A8I6B inhibits a count latching pulse and prevents an error count from being displayed. A8I17B will be set by the MASTER RESET pulse thus permitting the succeeding center passband counts to be displayed. The removal of the HI reset input to A8I17A ensures that the flip-flop will be set on the MASTER RESET pulse and will remain set. This disenables the last three frequency counter stages until A8I17A is clocked to a reset state by the 1,000th count output from the frequency counter. A8I6A is used as an inverter for the 1,000th count signal (A7I1 overflows output). This action subtracts 1,000 from the count displayed and compensates for a 445 kHz signal being used in place of the 455 kHz 2nd I.F. signal. The inputs to A8I25B with A8I16A set, gates the 445 kHz signal to A8I26B.

6.4.7 Frequency Counter and Display

The frequency counter and frequency LCD display are located on board A7. A7I1 and A7I2 are three digit multiplexed, decimal counters. The two counters operate in cascade and the overflow output of A7I1 is used by A8 to subtract 1000 counts when the CENTER PASS BAND frequency is to be displayed. A7I3 through A7I8 are latched decoders used to drive the LCD display. The phase control input to these decoders enables the AC signals required for an LCD display to be generated. NOR gate A7I9B inverts the multiplexing clock input to the counters and provides a strobe input to NOR gates A7I9A, A7I9C and A7I9D. The three NOR gates invert the digit designating signals from A8I1 and provide the latch input to the decoders for latching the decoder count inputs. Resistor A7R1, in conjunction with the gate input capacitance, delays the arrival of a LO input to the gates until after the multiplexed count outputs have reached their final state.

XOR gates A7I10 are used to drive the SIGNAL COUNT, AFC and decimal point inputs to the LCD display. Whenever the control input to the gate is HI, the LCD clock signals will be inverted by the gate and the associated indicator will be turned on.

HD1 is a self regulating heater, used to supply heat for low temperature operation (below −5.0°C) of the LCD display.

CHAPTER 7
LEVEL, DEMODULATOR AND POWER CIRCUIT THEORY

7.0 INTRODUCTION

This chapter will discuss the level output circuitry contained on boards A21, A22, A23 and A24, demodulation and audio output circuitry on board A5 and power supply and power control circuitry contained on boards A1 and A22.

A21, A22 and A23 schematics are shown in figure 12-5. The A5 and A1 schematics are shown in figure 12-2. The A24 schematic is shown in figure 12-1.

7.1 DIGITAL LEVEL OUTPUT CIRCUITRY

Figure 7-1 shows a functional block diagram of those circuits used to provide level outputs. The operation of these blocks will be discussed in the paragraphs to follow.

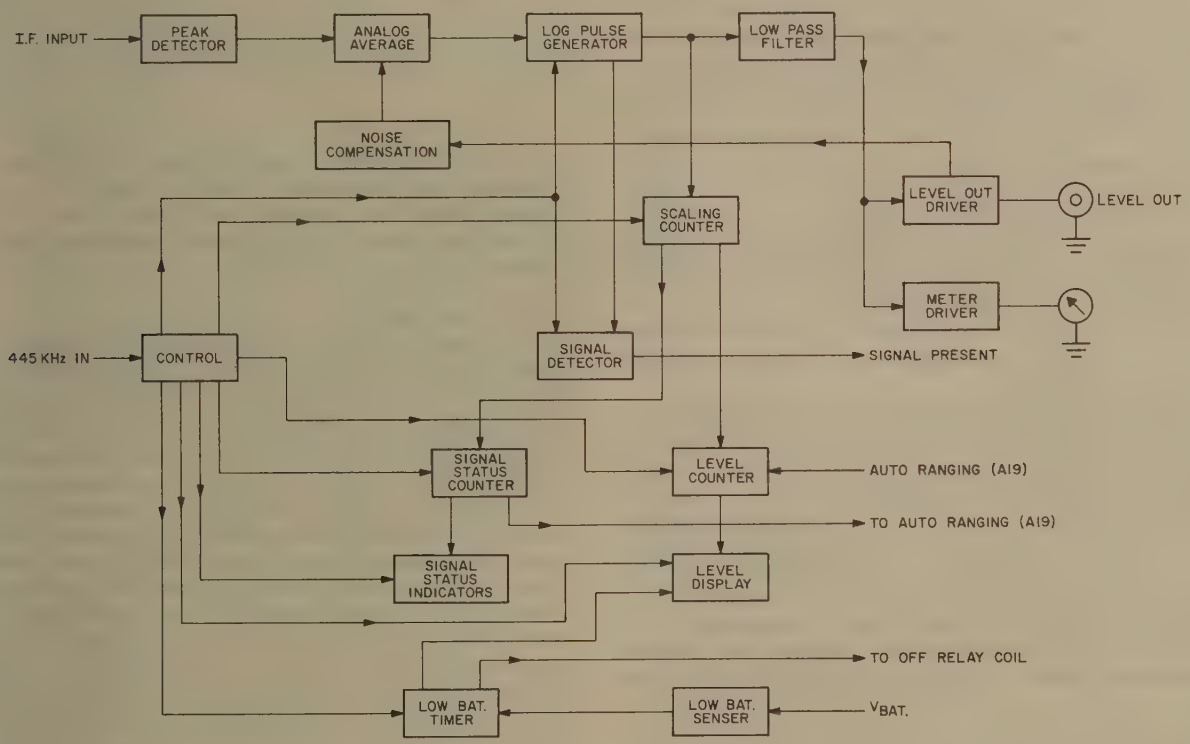


FIGURE 7-1
LEVEL OUTPUTS GENERATION

7.1.1 Peak Detector

The peak detector block consist of A21I1, A21I2 and A21I16. The I.F. input to comparator A21I1 is AC coupled with the 5 V regulator A21I16 providing the DC bias voltage. The inverting input to A21I1 will follow the peak voltage of the I.F. signal. Anytime the I.F. signal at A21I1 pin 3 exceeds the pin 2 level, the comparator output will increase the voltage stored on capacitor A21C2. Operational amplifier A21I2 is connected as a voltage follower and provides a high input impedance buffer between A21C1 and the circuitry that has to be driven. Resistor A21R4 provides discharge resistance that allows the capacitor voltage to decrease with a decreasing I.F. signal level. The detector DC output is referenced to the A21I16 output voltage and will equal the regulator voltage for a zero voltage input signal. Variable resistor A21R3 is factory adjusted to compensate for any offset error generated within the peak detector circuitry.

7.1.2 Analog Average

In order to obtain a stable level display, the signal provided by the peak detector requires averaging to remove any low frequency noise components that may be present. This averaging is accomplished, in part, by resistor A21R6 and capacitor A21C30. The 1 K resistor and 100 ufd capacitor provide a 0.1 second time constant.

7.1.3 Noise Compensation

Because of the relatively high amplitude resolution of this instrument, small level reading errors can result from internally generated noise depending upon bandwidth and signal level. These intrinsic noise generated errors have been corrected by the provision of controlled DC LEVEL OUT signal feedback which controls the value of the detector output level. The feedback voltage will have a DC level below the A21I16 output level and will subtract from the detector level. The subtracted voltage will increase for lower level readings.

When the unit is operating in a wide selectivity mode, variable resistor A21R40 will be shorted out by SELECTIVITY switch S3. Variable resistor A21R8 will control the amount of LEVEL OUT

signal feedback. Transistor A21Q6 simply reduces the load placed on A21I14B permitting the A21I14B output to drop to a lower minimum voltage. The variable resistors on board A24 permit the feedback voltage to be controlled by the position of the IMPEDANCE switch A2S2. The I.F. gain of the unit changes with the selection of different impedances and in turn requires a change in noise compensating feedback.

When the unit is operating in a narrow selectivity mode, variable resistor A21R40 limits the feedback compensation. The lower noise generation in the narrow selectivity mode eliminates the need for A24 board control.

Where required, some units may employ resistor A21R42, multipellet diode CR1 or A21CR4 to provide a non-liner feedback characteristic.

7.1.4 Log Pulse Generator

The log pulse generator block consists of A21Q1, A21I3 and A21I8A circuitry. The signal at the cathode of diode A21CR1 is a 43.46 Hz square wave derived from A21I7 of the control block. During the HI interval of the signal at A21CR1, transistor A21Q1 will be turned on and the voltage at A21C30 will be supplied to A21C3. When the signal at A21CR1 goes to a LO state, transistor A21Q1 will turn off. With A21Q1 off, capacitor A21C3 will discharge through resistors A21R11 and A21R12 to the +5 V level. The +5 V level corresponds to the zero signal level. Flip-flop A21I8A is reset at the same time A21Q1 is turned off and the A21C3 discharge begins. A21I8A is set by a HI output from comparator A21I3. The A21I3 output will go HI when A21C3 discharges below a threshold voltage, nominally 0.1 V above the zero signal level voltage (+5 V). Since an RC discharge curve is logarithmic, the time required for A21C3 to discharge to the threshold voltage will be proportional to the logarithm of the ratio of the detected voltage supplied to A21C3 and the threshold voltage across A21R14.

The $\overline{Q}$ output of A21I8A will be HI for the time required for A21C3 to discharge to the threshold. By using the HI output from A21I8A-$\overline{Q}$ to gate clock pulses to the scaling counter, a level count proportional to the HI state time of the A21I8A-$\overline{Q}$ output is generated. Variable resistor A21R11 provides control of the time constant for the A21C3 discharge. By adjusting the time constant in accordance with the frequency of the clock signal gated to the scaling counter, the level counts generated will indicate the ratio of the detected signal to the threshold level in tenths of a dB.

The log pulse generator output at A21I8A-$\overline{Q}$ will generate pulse widths of 359.6 microsecond per dB at a pulse rate of 43.46 Hz.

7.1.5 Control

The control block generates the various signals needed to generate and display a level reading. These signals are generated by counting and decoding the 445 kHz signal derived from the TCXO and decade counter A8I24. In earlier units having Serial Numbers 101 through 200, the 4.45 MHz signal was divided by 10 using a decade counter A21I5.

The control block consists of counters A21I6, A21I7, A21I12B, flip-flop A21I10A and gates A21I4C and A21I4D.

A21I6 is a 14 stage ripple counter. The Q4 output is the 445 kHz clock input divided by 16. Q4 provides a 27.8125 kHz clock signal to the scaling counter through gate A21I4A.

The Q10 output of A21I6 is 434.57 Hz and is used to clock counter A21I7. The Q13 output is 54.32 Hz and is used as a clock signal for the level LCD display.

Decade counter A21I7 has decoded outputs plus a square wave carry output. The carry output is used as a control signal to turn ON and OFF A21Q1 of the log pulse generator block. Decoded count output Q5 clocks A21I8A of the log pulse generator and the signal detector A21I8B. A21I7 count outputs Q1 and Q3 are gated with A21I10A outputs to generate level count latching and presetting signals. The Q1 signal is also used to clock counter A21I12B. The count output Q0 is used to set flip-flop A21I10A after preset and latch pulses have been generated.

Counter A21I12B is a modulus 16 binary counter. Output Q4 is a 2.72 Hz square wave. The rise of Q4 clocks and resets flip-flop A21I10A. With A21I10A reset, AND gates A21I4C and A21I4D are enabled. With a Q1 output from A21I7, a LATCH pulse is generated at the output of A21I4D. On a Q3 output from A21I7, a PRESET pulse is generated at the output of A21I4C. On a Q0 output from A21I7, flip-flop A21I10A is set.

The A21I12B-Q4 output is also used as the clock input to the LO BAT. timer A21I13, the reset input to A21I15 of the signal status counter and as drive to the base of A21Q5 of the Signal Status Indicator block.

7.1.6 Scaling Counter

The Scaling Counter consists of AND gate A21I4A and the four bit binary counter A21I12A. The control input to AND gate A21I4A is driven by the LOG PULSE output $\overline{Q}$ of A21I8A. When the LOG PULSE is HI, clock pulses from A21I6-Q4 are gated through to the clock input of A21I12A. The Q4 output of A21I12A drives the clock input of the level counter on board A22. The Q3 output of A21I12A will have twice as many output pulses as Q4 and is used as the clock input to A21I15 of the Signal Status Counter. The Signal Status Counter is active only during the second half of a level count interval and therefore, requires a times-two clock rate. A21I12A is reset by the level count PRESET pulse.

7.1.7 Level Counter

The Level Counter consists of the digital I.C.'s A22I1 through A22I4 on the A22 board. One XOR gate located on A23 is used as an inverter to complete the counter circuitry. A22I1, A22I2 and A22I3 are BCD presettable up/down counters, connected in cascade to form a three digit decimal counter. At the end of each count interval, the LATCH pulse latches the level count into latches located in the level display block. Following the latch process, the PRESET pulse sets the A22 counters to a starting count. The starting count is determined by signals provided by the Auto Ranging circuit board A19. These signals indicate the amount of attenuation provided by the unit attenuator and the level which corresponds to the threshold of the log pulse generator. Clock pulses provided by the Scaling Counter correspond to 0.1 dBm per pulse and the number of pulses for a level count interval indicates the amount by which the detected signal level exceeds the threshold level for the selected level range. When the starting level is negative, the counters will operate in a count down mode. When the starting count is positive, or when, during a count, the zero count state is reached, the counters will operate in an up count mode. The up/down count control line is driven by the Q output A22I4A which is clocked by the PRESET pulse. The E line signal from A19 drives the D input to A22I4A. A HI D input means that the flip-flop will be clocked to a set (up count) state. When the counters are in an up count mode, the LO $\overline{Q}$ output from A22I4A will preset the two least significant decimal digits to a 01 rather than a 99 condition.

If an all zero count is reached during the count interval, an active LO output from the carry out output of A22I3 will be inverted by A23I1B and will set A22I4A to the up count state. Resistor A23R1 and capacitor A23C1 act as a lowpass filter and prevent any spike that could be generated at the carry out output from A22I3 during the presetting process from causing A21I4A to be set.

The state of flip-flop A22I4B controls the positive sign LCD indicator segment. A22I4B is clocked by the LATCH pulse and

will be set whenever the completed count ends with the up/down signal in a HI up count state.

7.1.8 Level Display

The LCD level display and the display driving circuits are located on board A23. A23I2, A23I3 and A23I4 are LCD display drivers. These I.C.'s contain latches to store a completed count, BCD to seven segment decoding gates and phase control XOR gates used to generate the required AC outputs. XOR gates A23I1A, A23I1C and A23I1D drive the positive sign segment, LO BAT indicator and the negative sign segment inputs to the LCD display. When the control input to a gate is HI, the 54.3 Hz clock input to the gate will be inverted at the output and the driven LCD segment or indicator will be visible.

7.1.9 Signal Detector

The signal detector consists of flip-flop A21I8B. A21I8B is clocked at the same time A21Q1 is switched OFF. If the detected voltage on A21C3 is above the threshold level, the output of A21I3 will be LO. The LO input to A21I8B means the flip-flop will be reset, providing a HI output from the $\bar{Q}$ output or A21E11.

The A21E11 signal is used to enable SIGNAL COUNT and AFC modes of operation.

7.1.10 Signal Status Counter

The signal status counter generates signals indicating the extent to which a detected signal is above the log pulse generator threshold. One signal is provided to the Auto Ranging board (A19) indicating an attenuation change is required, while a second signal indicates whether an increase or decrease of attenuation is needed.

The signal status counter block consists of A21I15, A21I9A, A21I9B, A21I10B and A21I4B. Decade counter A21I15 is the input (0.1 dB) stage of the signal status counter. A21I15 is held in a reset state during the first half of a level counter interval by a HI input from A21I12B-Q4. If an automatic attenuation change takes place, the signal level being detected will probably be in a state of change during this first half of the level count interval. When the reset input goes LO, A21I15 is clocked at a rate twice that of the level counter input by the Q3 output of A21I12A. A21I9A and A21I9B are cascaded decade counters clocked by the count 9 output of A21I15. Flip-flop A21I10B is used for count decoding.

The PRESET pulse for the level counter is also used to reset the A21I9A, and A21I9B counters as well as A21I10B. This means A21I10B will remain set from count 0 until count 10 of the A21I9 counters is reached. On count 10 a HI input from Q1 of A21I9B will reset A21I10B.

A21I10B will remain reset between valid level counts 10 to 21. On count 20 the reset input to A21I10B will be removed. On count 21 the rise of the Q1 output of A21I9A will clock A21I10B to a set state. Whenever A21I10B is set, AND gate A21I4B is enabled. LATCH pulses provided to the level display will also be gated as a clock input to the Auto Ranging board, indicating an attenuation change is required. Additionally, the Q2 output of A21I9B is provided to the Auto Ranging board where a HI state will indicate that the change required represents an increase in attenuation.

7.1.11 Signal Status Indicators

The signal status indicators block consist of flip-flops A21I11A and A21I11B, transistors A21Q3, A21Q4 and A21Q5, and light emitting diodes A23CR1 and A23CR2.

Both A21I11 flip-flops are clocked at the end of a level count interval by the rise of the A21I10A-$\bar{Q}$ output. If the level count lies within the valid range, A21I11A will be clocked to a set state and A21I11B will be clocked to a reset state. In these states, both indicators will be turned off. When the level count exceeds 210 counts or +21 dBm, A21I11B will be set as a result of a HI D input from A21I10B. The HI set input to A21I11A from A21I9B-Q2 will prevent A21I11A from being reset. With A21I11B set, the red LED A23CR1 will flash, indicating that an over-range signal has been detected. Operationally, this is a demand for more signal attenuation to be inserted. The HI output from A21I11B-Q will provide a blanking input to the level display.

When the level count falls below 100 or +10 dBm, A21I11A will be reset. With A21I11A reset, A21I11B is held in a reset state by the HI reset input from A21I11A-$\bar{Q}$. With A21I11A reset, the yellow LED A23CR2 will flash indicating the level count does not lie in the accurate portion of the detection window. Operationally, this is a demand for a reduction of signal attenuation by a 10 dB step.

Transistors A21Q3 and A21Q4 provide current gain, allowing the LED's to be driven by CMOS outputs. Darlington transistor A21Q5 is controlled by the 2.7 Hz A21I12B-Q4 signal. The commutation of A21Q5 results in the flashing of the LED indicators.

7.2 ANALOG LEVEL OUTPUTS

The lowpass filter, level out driver, and meter driver, blocks are used to provide analog level outputs for various purposes.

7.2.1 Low Pass Filter

The low pass filter consists of operational amplifier A21I2A and its associated circuitry. The A21I2A circuit is in a conventional non-inverting low pass active filter configuration. The gain factor is 1.28. The circuit converts the positive going log pulses at A21I8A-$\bar{Q}$ to an average DC voltage. The output of A21I2A will nominally be 1.0 volt per 5.0 dBm of detected signal above the level threshold.

7.2.2 Level Out Driver

The level out driver block consist of operational amplifier A21I14B. A21I14B drives the LEVEL OUT BNC terminal. The circuitry associated with A21I14B provides a lowpass non-inverting configuration with a 1.0 gain factor. The driver circuitry further reduces the ripple present at the A21I2A output. The 2.0 K resistor A21R24 protects the driver from the effects of possible shorted external loads.

7.2.3 Meter Driver

The meter driver block consists of A21I14A. The circuitry is configured for current output. The voltage across A21R29 will nominally be 5.1 times the voltage difference between the A21I2A output and the A21E18 voltages.

With the METER REF. switch S1 in the IN position, A21E18 will be grounded and A21E17 and A21E16 will not be connected. In this configuration, the meter range corresponds to the 21 dBm range of the digital level readings.

With the METER REF. switch S1 in the OUT position, resistor A21R31 is connected in parallel with A21R29 increasing the driver current gain. The voltage at A21E18 with the switch OUT is adjustable and is controlled by adjusting R1. In this mode, the meter has about a 4.0 dBm range and can be adjusted with the METER REF. control R1 to place an arbitrary operator selected reference reading in the center of the meter.

7.3 DEMODULATOR

Demodulator circuitry is contained on board A5. The A5 schematic is located in figure 12-2.

The demodulator input from the I.F. assembly may be either an unmodulated or an amplitude-modulated signal. For AM signals, A5Q1 and A5Q2 are disabled by the DEMODULATOR switch A5S1 which disconnects their supply voltage. For amplitude modulation, the cathode of A5CR2 is grounded through A5S1. A5CR2 is employed as a shunt type detector which rectifies

the incoming 455 kHz signal at A5E8. Lowpass filtering by A5R12 and A5C8 removes the I.F. frequency component allowing the audio modulation to reach the audio amplifier stage through the DEMODULATOR LEVEL control R4.

Carrier reinsertion oscillator A5Q1 output is mixed with the I.F. signal in both upper (USB) and lower sideband (LSB) position of A5S1. This produces an aural audio difference frequency output. A5Q1 is a FET oscillator in a Pierce configuration whose output frequency is determined by the selection of A5Y1 or A5Y2. LSB crystal A5Y2 is fixed at 1.5 kHz below the frequency while crystal A5Y1 is fixed at 1.5 kHz above the I.F. frequency. A5Q2 is a phase-splitter generating two signals 180° apart for a balanced shunt demodulator consisting of A5CR1 and A5CR2. The shunt demodulator shorts the 455 kHz I.F. input to ground during one-half of the injection cycle. Signal components appearing at the anode of A5CR2 include an audio difference component. The higher frequency components are by-passed to ground by A5C8 and the audio beat frequency is coupled to the audio amplifier input.

Audio amplifier A5I2 consists of a single integrated circuit package. The amplifier is connected in a bridge configuration with both outputs isolated from ground and the loudspeaker load bridged between the two output terminals. Because the two outputs are 180° phase apart, the output voltage swing can be doubled in a bridge configuration. The output from A5I2A is in phase with its input and its gain is determined by resistor values A5R13 and A5R14. The A5I2B input is derived from A5I2A through A5R14. A5I2B is an inverting amplifier supplying the opposite side of loudspeaker LS1. Typical voltage gain of the audio amplifier is 48 dB.

7.4 POWER

The unit power system consists of the Power Supply Assembly A15 which contains the power supply board A1 along with the power transformer A15T1, bridge rectifier A15CR1 and AC line fuse A15F1, auto/off circuitry on boards A22 and A21, three terminal regulators on various boards throughout the unit and the unit POWER switch S2.

A15, A1 and S2 schematics are found in figure 12-2. A22 and A21 schematics are found in figure 12-5.

7.4.1 Battery Charging

With the POWER switch S2 in the CHARGE position, all the AC input power is used in charging the unit battery.

Transformer A15T1, bridge rectifier A15CR1 and capacitor A1C1 form a conventional AC to DC converter.

The positive 5 volt regulator A1I1 provides the charging voltage to the battery via the power diode A1CR1 and switch S2. The resistance network of A1R1, A1R2 and A1R7 determine the voltage at the common, normally grounded, terminal of A1I1. A1R2 is adjusted such that about 14.1 volts will be present at the cathode of A1CR1 with the transistor A1Q1 turned off and with about a 360 mA load current. The 2.0 ohm resistor A1R8 provides a sense of the amount of charging current being accepted by the battery. If the battery draws more than 300 mA of charging current, transistors A1Q2 and A1Q1 will be turned on by the voltage across A1Q2. The collector current of A1Q1 will flow through resistor A1R7, raising the common terminal and the output voltage of the regulator. Resistor A1R5 limits the A1Q1 collector current and holds the maximum charging voltage to about 15.1 volts. Since the charging voltage will drop back to a trickle charge level (14.1 volts) when the battery becomes fully charged, rapid charging can be accomplished without the danger of an overcharge.

Diode A1CR1 prevents the loss of battery current through the charging circuitry when the unit is operating without AC power.

7.4.2 POWER ON

When the POWER switch S2 is moved from the CHARGE to the ON position, relay A22K1 is pulsed to the ON state. The operation of A22K1 will be discussed in more detail in the Auto/Off section 7.4.4. When A22K1 is in an "on" state, battery voltage at A22E2 is connected to A22E4. A22E4, in turn, supplies the battery voltage to the A1 board. The A1 regulator A1I3 supplies 10 V regulated power to A5, A7, A8 and A11. The regulator A1I2 supplies 10 V regulated power to A21, A22 and A23. Connections on the A1 board provide for the distribution of battery voltage to the remaining boards of the unit. These boards contain their own 10 V or 8 V regulator.

The power distribution system also contains a number of feed-through capacitors and inductors comprised of ferrite beads located on various power leads. These components eliminate the coupling of high frequency signals between boards through the power system.

With S2 in the ON position, the base and emitter leads of A1Q1 are shorted together holding A1Q1 shut-off. This means that the cathode of A1CR1 will remain at a trickle charge voltage condition.

7.4.3 BAT. TEST

With S2 in the BAT. TEST position, AC power is disconnected from the power transformer A15T1. Terminal A21E20 will be grounded via S2, thus holding off any current output from A21I14A. S2 will supply battery voltage to A21E25. The difference voltage between the regulated voltage at the base of A21Q2 and the battery voltage at A21E25 determines the collector current of A21Q2. Diode A21CR2 directs A21Q2 collector current through the meter. Variable resistor A21R46 is factory adjusted such that the meter will read at the bottom edge of the BAT. OK area when the unit is about to enter a LO BAT. mode of operation, (battery voltage approx. 11.8 V). On units Serial Numbers 101 to 200, a selected A21R34 was used in place of A21R46.

7.4.4 Auto/Off

Latching relay A22K1 provides the means for automatically turning off the unit when the battery voltage reaches a minimum limit. This prevents a deep battery discharge which might otherwise damage the battery.

When S2 is in a CHARGE position, relay A22K1 will be in a reset state with all contacts open. Terminal A22E1 will be grounded through S2 and A22E2 will be connected through S2 to battery voltage. If A22K1 had been set prior to the movement of S2 to the CHARGE position, current will flow through A22CR3 and the reset coil of A22K1 would pulse the relay to the reset state.

With A22E1 at ground and A22E2 at battery voltage, capacitors A22C1 and A22C2 will be charged to the battery voltage through A22CR2 and A22R1. When S2 is now moved to the ON position, S2 will short together and place both A22E1 and A22E2 at the battery voltage. Capacitors A22C1 and A22C2 will discharge through A22CR1 and the set coil of A22K1, pulsing this relay to the set condition with contacts closed.

Contacts 10 and 11 are used to supply operating power to the boards of the unit. Contacts 4 and 5 supply power to the reset coil of the relay and to the display self-regulating heaters. Contacts 3 and 2 provides a connection between the battery and the AUX+12V jack at the lower left hand corner of the front panel.

The resistor network consisting of A22R2, A22R3, A22R4 and A22R5 supply a portion of the battery voltage to the non-inverting input of comparator A22I5B. As long as the battery voltage input to A22I5B remains above the threshold input provided by the A22R6 and A22R7 voltage divider, a HI output from A22I5B will hold the binary counter A21I13 in a reset state. Variable resistor

A22R3 is adjusted such that when the battery voltage drops below 11.8 V, the A22I5B output will go LO. With a LO reset, input counter A21I13 will count at the 2.7 Hz rate of the clock input.

The first stage Q1 output of the counter activates the LO BAT. indicator of level LCD display. This will alert the user that the Auto/Off counter has been activated. Any time S2 is returned to a CHARGE position, and then back to the ON position, the action of capacitor A22C3 and diode A22CR5 will guarantee a short term HI output from A22I5B. This HI pulse will reset the A21I13 counter. When not reset, the A22I13 output Q13 will go HI after 4096 counts, the equivalent of 25.28 minutes. A HI output from A22I13-Q13 supplies base drive to the Darlington transistor A22Q1 activating the reset coil of A22K1. With A22K1 reset, the unit is turned OFF pending battery re-charge or manual reset operations.

7.4.5 AUX +12V

With A22K1 in the set, ON state, the AUX +12V jack on the front panel is connected to the positive battery terminal. 1.0 ohm resistor A1R10 limits the current flow through the jack. Power may flow through the jack in either direction. Unit power may be used to power an external probe through this jack, or a car battery may be used to inject power to the unit. In the case where external power is being supplied to the unit, the internal battery is still required to provide the pulse needed to set relay A22K1, i.e. operation of the unit without an internal battery being present is not possible.

7.4.6 Fuses

A 2 Amp fuse A1F1 protects the battery from excessive current resulting from a short circuit. The AC line is fused by A15F1, a ¾ Amp slo-blow fuse.

CHAPTER 8
MAINTENANCE

8.0 GENERAL

The first part of this chapter provides a procedure for calibrating and verifying the performance of a 6040 unit. The procedure will be followed by information that will aid in trouble shooting a faulty unit.

8.1 CALIBRATION AND VERIFICATION PROCEDURE

This procedure assumes that the operator has some familiarity with the Model 6040 and has a good general understanding of test equipment. Except where indicated, all tests are made with the unit powered from the AC line. The figures of Chapter 10 will be helpful in locating components referred to in this procedure.

8.1.1 Test Equipment Required

The following is a list of equipment that may be used for 6040 testing. The substitution of equivalent pieces of test equipment for those shown is permissible. It must be borne in mind that the accuracy of an instrument is no better than the accuracy of the equipment used to calibrate that instrument.

A given test will be written for the equipment listed. When other equipment is substituted, the test operator is expected to make the necessary technical or procedural adjustments.

(i) 50 ohm ±1% BNC male to BNC female feedthrough termination — H.P. 10100C
(ii) Frequency Synthesizer — H.P. 3325A
(iii) Frequency Counter — H.P. 5335A
(iv) Analog Level Meter — Anritsu ML424A
(v) Digital VOM — Fluke 8050A
(vi) Oscilloscope — Tektronix 465 or 465B
(vii) Spectrum Analyzer — H.P. 3585A
(viii) Power Supply — Viz WP707
(ix) Power Resistors or Rheostat values as required
(x) Noise Generator — Marconi TF2091B with appropriate filters
(xi) 10:1 Probe — H.P. 10040A
(xii) VHF Attenuator — H.P. 355B and H.P. 355C combined
(xiii) Active Probe — H.P. 1120A
(xiv) Coaxial Series Resistor 27 ohm

8.1.2 Removal of Case

For the majority of tests in the procedure it will be necessary for the unit to be uncased before internal connections or adjustments can be made. Unless otherwise stated, the tests assume that the unit is uncased.

The case is secured to the unit chassis by four Philips head screws. Two screws are on the top and two on the bottom of the unit adjacent to the front panel casting. After these four screws have been removed, the chassis can be withdrawn from the case.

8.1.3 Power Supply and Charging Control

(a) Set the POWER switch to OFF and insert the AC power cord. Place the unit on its back and disconnect the battery.

(b) Connect one clip lead to A1E1 (the positive battery lead terminal) and a second clip to the chassis. These two leads are to be used for connecting test loads item 8.1.1 (ix) to the unit.

(c) Connect a 200 ohm 2 W resistor as a test load. Set the POWER switch to ON. Adjust A1R2 for 14.10 to 14.20 V DC voltage across the test load. The unit should have stabilized at room temperature when this adjustment is made.

(d) Set the POWER switch to the CHARGE position and change the load resistor to a 20 ohm 20 W resistor. The voltage shall be 14.7-15.7 V DC.

(e) Change the load resistor to a 50 ohm 10 W resistor. The voltage shall be 14.7-15.7 V DC.

(f) Change the load resistor to a 200 ohm 2 W resistor. The voltage shall be 14.10-14.40 V DC.

(g) Connect a 50 ohm 10 W resistor across the battery leads. Verify that the battery voltage is 12.0 V DC minimum.

(h) Provided that the battery meets the step (g) requirement, set the power switch to OFF and reconnect the battery. If the battery voltage is low, replace the battery. (See NOTE 2. page 1-6 on disposal of batteries)

(i) Set the power switch to ON. Measure the voltages at J5-5 and J5-K. The voltage should be 9.5-10.2 V DC.

8.1.4 Initial I.F.

(a) Check the voltages at the outputs of voltage regulators A4I2 and A4I4 using digital VOM item 8.1.1 (v). The voltages should be 9.5-10.2 V DC.

(b) Disconnect the 1st L.O. cable connecting to A4J2. Check voltages at A4TP2 and TP3. The voltage at TP3 should be 5.0 ±0.3 V DC. Adjust the voltage at TP2 to match TP3 by adjusting A4R15.

8.1.5 Initial Input Selector Verification (Unbalanced Input)

(a) Set up the spectrum analyzer item 8.1.1 (vii) as follows:

(1) Press Instrument PRESET
(2) Turn Tracking Generator Amplitude Max. clockwise (0 dBm)
(3) Stop Frequency = 5 MHz
(4) dB/DIV = 1 dB/DIV
(5) 1 Megohm IMPEDANCE = ON (light on)
(6) AUTO RANGE = OFF (light off)
(7) REF LVL TRACK = OFF (light off)
(8) RANGE = 10.0 dBm

(b) Connect the equipment as shown in figure 8-1.

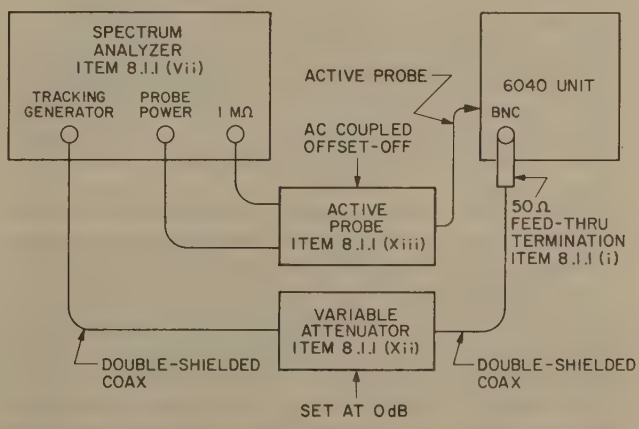


FIGURE 8-1
INPUT SELECTOR VERIFICATION HOOKUP DIAGRAM

(c) Set the unit switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−80 dBm
IMPEDANCE	50 ohm BRG
POWER	ON

(d) Connect the active probe to the BNC connection on the A2 board; ground the probe where the black banana jack is soldered to A2. Adjust the reference level on the analyzer for a trace located in the center of the screen.

(e) Adjust the spectrum analyzer as follows:

(1) Push STORE A→B button.
(2) Push A-B button. Light should turn on.
(3) Push VIEW B button. Light should turn off.
(4) Push OFFSET button. Light should turn on.
(5) Push ENTER OFFSET button.

(f) Connect the active probe to the capacitor (A2C3) lead next to A2J1. The displayed signal should be flat from 0 to 5 MHz; compare this against the display line by pushing the DSPL LINE button (the light should turn on) and by rotating the knob located just to the right of the OFF button until the display line is about 0.1 dB away from the displayed signal. There should be a constant gap between the two curves.

(1) Push the A-B button (the light should turn OFF).
(2) Push the CLEAR button just to the right of the DSPL LINE button. The DSPL LINE light should turn off and the display line should disappear.
(3) Push the MARKER button.
(4) The OFFSET reading on the display (upper right hand corner) should read 0.00 ±0.10 dB.

8.1.6 Initial Attenuator/Summing Amplifier and Common Mode Rejection

(a) Disconnect the attenuator/summing amplifier output cable that plugs into A4J1. Connect the active probe and its ground to the end of this cable. Adjust the reference level on the analyzer for a trace located in the center of the screen. The OFFSET reading on the display should read −5.30 ±0.30 dB. Push the A-B button and compare the curve to the display line in a manner similar to step 8.1.5 (f). There should be a constant gap between the two curves.

(b) Change the 6040 from the UNBAL to BAL input mode. Remove the input cable and 50 ohm load from the UNBAL BNC input jack. Connect them to a female BNC-to-male banana adapter. Insert the adapter into the two blue banana jacks on the 6040, with the ground side going to the center banana jack. The top blue banana jack is referred to as E1. The center blue banana jack is referred to as E2. The black banana jack is ground. Connect E2 to ground with a very short jumper wire. In a similar fashion to step 8.1.6 (a), look at the unloaded attenuator/summing amplifier cable output that plugs into A4J1. The OFFSET reading should be within ±0.05 dB of the reading observed in 8.1.6 (a). Compare the curve to the display line as done previously in step 8.1.6 (a); there should be a constant gap between the two curves.

(c) Move the banana adapter to the center blue and black banana jacks, with the ground side of the adapter connecting to the black banana jack. Remove the short between E2 and ground. Connect E1 to ground with a very short jumper wire. In a similar fashion to step 8.1.6 (a), look at the unloaded attenuator/summing amplifier cable output that plugs into A4J1. The OFFSET reading should be within ±0.10 dB of the reading observed in 8.1.6 (a). Compare the curve to the display line as done previously in step 8.1.6 (a). The maximum variation between curves should not exceed ±0.1 dB at any frequency between 0 and 3.5 MHz.

(d) With the same electrical hookup used in 8.1.6 (c), adjust the spectrum analyzer 8.1.1 (vii) as follows:

(1) Push A-B to OFF position
(2) MARKER to ON position (should be at horizontal center of screen)
(3) dB/DIV = 10 dB
(4) Push MKR→REF LVL button until trace stays in same position at top of screen.
(5) Check to make sure that the OFFSET button light is ON.
(6) Push ENTER OFFSET button.

Now remove the short between E1 and ground on the 6040. Using a very short jumper wire, short E1 and E2 together. Adjust the RANGE on the spectrum analyzer to −5.0 dBm. Adjust capacitor A3C15 for the lowest curve (minimum reading) on the spectrum analyzer. The common mode rejection should be at least 30 dB down at 250 kHz, and 20 dB down at 1 MHz. Remove the short between E1 and E2.

8.1.7 Low Pass Filter (LPF) Adjustment

(a) Repeat steps 8.1.5 (a) through 8.1.5 (e).

(b) Connect the active probe to A4TP1 and ground the probe on the outer jacket of the 1st L.O. cable that connects to A4J2. Adjust the REF LVL on the spectrum analyzer for a trace where the 0 Hz frequency is vertically centered in the display. Turn off the A-B and OFFSET buttons on the spectrum analyzer (light off). Adjust the marker to 250 kHz. Turn on the OFFSET button; the offset level reading should be −12.80 ±1.00 dB.

(c) Disconnect the two local oscillator cables connecting to A4J2 and A4J3. Make sure the double-shielded cable that connects to the 6040 UNBAL input is also grounded to the 6040 chassis with a good electrical/mechanical connection somewhere along the cables length. Connect the active probe ground to the chassis right next to A4L3. Set up the spectrum analyzer as follows:

(1) Push the SAVE (OFF) and 1 REG buttons.
(2) CENTER FREQUENCY = 5.247 MHz
(3) FREQUENCY SPAN = 1 MHz
(4) RES BW = 10 kHz
(5) VIDEO BW = 1 kHz
(6) REFERENCE LEVEL = −85 dBm
(7) RANGE = −25.0 dBm
(8) dB/DIV = 2 dB/DIV

(d) Adjust the A4L1 and A4L5 coils 4 complete turns below where they hit the top of the coil cans. Adjust A4L2 for a null at 5.25 MHz. Change the spectrum analyzer center frequency to 5.46 MHz. Adjust A4L3 for a null at 5.46 MHz. Change the spectrum analyzer center frequency to 7.42 MHz. Adjust A4L4 for a null at 7.42 MHz.

(e) Press RECALL (on) and 1 REG buttons on the spectrum analyzer. Push the A-B button (the light should turn on). Use the display line as a reference straight line, and adjust coils A4L1 through A4L5 to obtain a flat response (±0.05 dB) between 0 and 3.25 MHz. Also adjust for a roll off of −0.25 ±0.05 dB at 3.5 MHz. Avoid adjustment of A4L2, L3, and L4 very far from their original settings in step 8.1.7 (d).

(f) Adjust the spectrum analyzer as follows:

(1) Push A-B button (light should turn off)
(2) Turn display line OFF, by pressing the CLEAR button.
(3) Push the OFFSET button. (light should turn off)
(4) Move marker to 2.5 MHz.
(5) Push MKR→REF LVL until trace is stable at top of screen.
(6) Push OFFSET button (light should turn on)
(7) STOP FREQ = 10 MHz
(8) dB/DIV = 10 dB/DIV
(9) RANGE = −15.0 dBm

The OFFSET reading should be less than −50 dB. After the first notch occurs in the stop band, the rest of the stop band should be at least 70 dB down out to 10 MHz. Reconnect the 1st and 2nd L.O. cables to the I.F. board.

8.1.8 Initial Cal Level Control Centering

(a) Adjust the CAL LEVEL potentiometer to its mechanical center by measuring the center tap voltage and setting it at 5.00 V DC.

(b) Adjust the potentiometer A4R108 for a voltage reading at the junction of A4R107 and A4R104 of 4.28 V DC.

8.1.9 TCXO Adjustment

NOTE: The TCXO should only be adjusted after the unit has been on for more than 30 minutes and is operating in an ambient temperature of about 23°C. (The frequency cover assembly A6 may be removed at this time)

(a) Access to the reference oscillator (TCXO) signal can be obtained at A8TP1. (If the frequency assembly cover is not removed, the hole on the top side of the cover provides access to the TCXO signal.) The frequency should be monitored using a 10:1 scope probe and counter item 8.1.1 (iii).

(b) Remove the screw on the side of the TCXO to obtain access to the frequency adjustment. With an insulated hex tuning tool, adjust the TCXO frequency to 4,450,000 Hz. Set the frequency such that the lower order digits agree with the SET TO frequency stamped on the TCXO module.

8.1.10 2nd L.O. and 4,545,000.0 kHz Loop Check

NOTE: If the frequency cover assembly was not removed in Test 8.1.9, remove it at this time.

(a) Remove the 2nd L.O. input to A8E4. Connect to A8E4 frequency synthesizer item 8.1.1 (ii). Use a sine wave 4.0 V p-p input signal at about a 5.0 MHz frequency. With a scope and probes item 8.1.1 (vi) monitor the signals at A11I8 pin 1 and A11I8 pin 4. A 9 to 1 division should be observed between the I8 pin 1 and I8 pin 4 signals.

(b) Increase the A8E4 input signal frequency. The 9 to 1 division should be maintained with a frequency increase up to 7.0 MHz.

(c) Disconnect the frequency synthesizer input and reconnect the A8E4 input from the 2nd L.O.. Monitor the A8E4 input with the scope item 8.1.1 (vi) with probe. The A8E4 signal should have a greater than 7.0 V p-p signal level.

(d) Add frequency counter item 8.1.1 (iii) to the scope output. The frequency of the 2nd L.O. signal should be 5,454,000.0 ±0.5 Hz.

(e) Using the digital VOM item 8.1.1 (v) monitor the DC voltage level at A11E4. This voltage level should lie between 6.0 V and 8.0 V.

(f) Monitor the signal at A8R11 at the resistor end opposite A8I28. Note the pulse widths of the shortest positive and negative pulses. These pulse widths should be about equal. If positive pulses are longer add a 100 K resistor A8R12 connecting the power end to point B, the +10 V line. If negative pulses are longer, add resistor A8R12 connecting the power end to point A ground. Verify that the addition of A8R12 has improved the symmetry of the A8R11 signal.

(g) Disconnect the 2nd L.O. output cable going to the I.F. Board J3 and connect the scope, item 8.1.1 (vi), to the end of the cable. The output signal should meet the following specifications:

Output:	Sine Wave (unloaded)
Output Level:	2.1 ±0.3 V p-p (unloaded)
Loaded Output Level:	1.0. ±0.2 V p-p (loaded with 33 ohms)

8.1.11 1st L.O. Adjustment and Check

(a) Use the scope item 8.1.1 (vi) with probe to monitor the A8 1st L.O. input at A8E2. The signal at A8E2 shall have a low level less than 0.3 V and a high level greater than 2.7 V. Add the frequency counter item 8.1.1 (iii) to the scope output to continue this test.

(b) Set the RANGE (frequency) switch to band 4 (2 − 3.5 MHz).

(c) Adjust the TUNE control to full CW for maximum frequency.

(d) Set A9L1 to display 8,550 kHz ±2 kHz on the external frequency counter.

(e) Rotate the RANGE (frequency) switch through the frequency bands and note the frequencies observed.

(f) Adjust the TUNE control full CCW for the lowest frequency and rotate the RANGE (frequency) switch. Note the frequencies.

TABLE 8-1.
FREQUENCY REQUIREMENTS

RANGE	Low Frequency (f.)	High Frequency (e.)
1-650	5,000 kHz	5,650 kHz
550-1650	5,550 kHz	6,650 kHz
1300-2400	6,300 kHz	7,400 kHz
2000-3500	7,000 kHz	8,500 kHz

(g) Step (e) frequencies should exceed the table frequencies and step (f) frequencies should fall below the table frequency. A9L1 may require additional adjustment in order to meet all the requirements.

(h) Disconnect the 1st L.O. output cable going to the I.F. Board J2 and connect the scope item 8.1.1 (vi), to the end of the cable. Set the 6040 frequency RANGE switch to the (2000-3500) band and tune to max. CW position. The output signal should meet the following specifications:

Output:	Square Wave
Duty Cycle:	50 ±2% (measured on center line)
Output Level:	1.2 ±0.2 V p-p (measured between flat portions)
RISE/FALL Time:	10 nanoseconds (measured between +0.4 V and −0.4 V levels)
Loaded Output Level:	0.6 ±0.1 V p-p (loaded with 27 ohms)

(i) Install A6 (Frequency Housing Cover Assy.) back in unit.

8.1.12 Initial Level Detector Adjustments

(a) Connect the digital VOM item 8.1.1 (v) reference lead to A21TP2 or A21E21. Connect the 2nd meter lead to A21TP1.

(b) Disconnect the I.F. input to A21E2. Connect the frequency synthesizer item 8.1.1 (ii) between A21E2 and ground. Provide a 2.70 V p-p 455 kHz input to A21E2. Note the digital VOM reading. The A21TP1 voltage should be about 1.35 V. Drop the synthesizer voltage by 20 dB and observe the change in the A21TP1 voltage. Adjust A21R3 to obtain a DC voltage that is 1/10 the higher voltage.

(c) Return the synthesizer to the higher level output and note the new D.C. voltage. Again drop the synthesizer level by 20 dB and readjust A21R3, if required. Continue the process until a 20

dB input level change generates a 10:1 change in the A21TP1 DC level. Disconnect the digital VOM 8.1.1 (v).

(d) Use a jumper to short together A21E21 and A21E24. Adjust A21R8 to the most CCW position. Set the RANGE dBm (MAX LEVEL) switch to the +10 dBm position.

(e) Adjust the synthesizer output level to obtain a +10.5 dBm level display. Reduce the synthesizer signal by 10 dB and note the level display reading.

(f) Return the synthesizer level to the previous +10.5 dBm level. Adjust A21R11 to obtain a level display reading of +10 dB above the reading noted for the down 10dB level input.

(g) Repeat steps 8.1.12 (e) and 8.1.12 (f) until level display readings of +10.5 dBm and +0.5 dBm are obtained for an input level change of 10 dB.

(h) With a level input providing a +0.5 dBm level display reading, reduce the input level 10 dB. Adjust A21R3 to obtain a −9.5 dBm level display reading.

(i) Return the input level up 10 dB and adjust the input level for a +0.5 dBm level display reading.

(j) Repeat steps 8.1.12 (h) and 8.1.12 (i) until a 10 dB reduction in level from the +0.5 dBm reading level provides a −9.5 dBm reading.

(k) Using the +0.5 dBm level as a pivot point, step the input level by +10 dB and −10 dB. Adjust A21R11 to correct the +10.5 dBm reading errors and adjust A21R3 to correct the −9.5 dBm reading errors. Each adjustment can effect all readings. A few iterations will be required, after which the level display reading will correctly track 1 dB level input steps over a 20 dB range.

(l) Connect a digital VOM item 8.1.1 (v) to the unit LEVEL OUT. Note the LEVEL OUT voltages for the corresponding level readings (Table 8-2).

TABLE 8-2
LEVEL OUT VOLTAGE

Level Reading	Level Out Voltage
−9.5 dBm	Less than 0.5 V
−7.5 dBm	0.5 V ±0.05 V
+0.5 dBm	2.1 V ±0.1 V
+10.5 dBm	4.1 V ±0.2 V

(m) Remove the frequency synthesizer signal to A21E2 and reconnect the I.F. input.

(n) At this point, the level display is capable of providing readings useable for adjustment of the other portions of the unit. Place A21R40 in the most CCW position and remove the A21E21 to A21E24 jumper.

8.1.13 I.F. Alignment

(a) Connect the equipment as shown in figure 8-2.

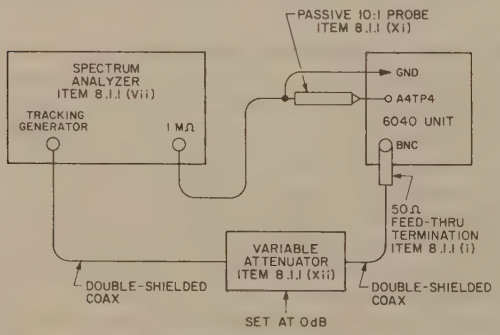


FIGURE 8-2
I.F. ALIGNMENT HOOKUP DIAGRAM

(b) Set up the spectrum analyzer item 8.1.1 (vii) as follows:
- (1) Press INSTR PRESET
- (2) Turn Tracking Generator Amplitude Max. Clockwise (0 dBm)
- (3) CENTER FREQUENCY = 455 kHz
- (4) FREQUENCY SPAN = 5 kHz
- (5) REFERENCE LEVEL = 5 dBm
- (6) dB/DIV = 10 dB/DIV
- (7) RES BW = 30 kHz
- (8) VIDEO BW = 100 Hz
- (9) Push 1 M ohm button (light should turn on)
- (10) Push AUTO RANGE button (light should turn off)
- (11) Push REF LVL TRACK button (light should turn off)
- (12) RANGE = 5.0 dBm

(c) Set the unit switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−10 dBm
IMPEDANCE	50 ohm BRG
CAL LEVEL	Mid range
SELECTIVITY	WIDE
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	455.00 kHz
AFC	OFF
POWER	ON

(d) Adjust A4T6, A4T5, A4T4 and A4T1 for a maximum response as viewed on the spectrum analyzer.

(e) Change the dB/DIV on the spectrum analyzer to 1 dB/DIV. Readjust A4T6, A4T5, A4T4 and A4T1 for a maximum response. Adjust the reference level on the spectrum analyzer as necessary to keep the trace centered.

(f) Change the SWEEP TIME on the spectrum analyzer from 0.2 sec to 0.8 sec. Readjust A4T6 and A4T1 for the best bandpass shape using the following criteria:

- (1) Maximum pass band ripple, 0.05 dB
- (2) Highest peak in center of pass band.
- (3) Shape of both sides symmetrical.

8.1.14 I.F. Gain and Scaling Verification

(a) Change the spectrum analyzer controls as follows:
- (1) dB/DIV = 2 dB/DIV
- (2) VIDEO BW = 10 Hz
- (3) SWEEP TIME = 1.6 sec
- (4) Push MKR→REV LVL until a stable trace is obtained at the top of the spectrum analyzer screen.

The marker level should read −3.0 ±3.0 dBm.

(b) Press the OFFSET button (light should turn ON). Press the ENTER OFFSET button. Observe the relative gain for the impedance switch settings listed in table 8-3, taking the readings from the OFFSET level on the spectrum analyzer screen.

TABLE 8-3
IMPEDANCE SWITCH/I.F.
RELATIVE GAINS

Impedance Switch Settings	Relative Gains
50 ohm BRG	0 dB
75 ohm BRG	−1.68 ±0.20 dB
124 ohm BRG	−3.74 ±0.20 dB
135 ohm BRG	−4.08 ±0.20 dB
150 ohm BRG	−4.52 ±0.20 dB
600 ohm BRG	−10.14 ±0.20 dB
600 ohm TERM	−11.02 ±0.20 dB
150 ohm TERM	−5.92 ±0.20 dB
135 ohm TERM	−5.60 ±0.20 dB
124 ohm TERM	−5.34 ±0.20 dB
75 ohm TERM	−4.12 ±0.20 dB

8.1.15 Initial AFC Check

(a) Set the unit switches and controls as follows:

Switch/Control	Position
RANGE dBm	CAL −30 dBm
IMPEDANCE	CAL
DISPLAY	CENTER PASS BAND
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
METER REF.	IN
CAL LEVEL	Mid-range
FINE TUNE	Mid-range

(b) Tune the unit to obtain a level reading for the 250 kHz signal.

(c) Adjust the tuning to obtain a level reading below the peak reading and near the lower end of the level range. The low level indicator should be flashing.

(d) Switch the AFC switch to the ON position. The switching action should result in a change in the frequency display, a peaked level reading and an AFC indication on the frequency display.

(e) With the frequency counter 8.1.1 (iii) and 10:1 probe 8.1.1 (xi), monitor the I.F. frequency at A21E2. The frequency should be 455,000.0 Hz ±0.2 Hz.

8.1.16 Cal Osc Adjustment

(a) Calibrate the Anritsu level meter 8.1.1 (iv) as follows:

(1) Turn the power switch OFF.
(2) Remove all input cables.
(3) Set the meter on a level surface where the unit will be used for making measurements.
(4) Adjust the mechanical zero of the meter, if necessary. The meter needle should be located directly above the furthest left scale marking on the NORM (bottom) scale.
(5) Turn the power switch ON.
(6) The unit should have a minimum 30 minute warmup time prior to the following steps.
(7) Push METER switch to EXP position.
(8) Push 0 dBm LEVEL CAL to ON position.
(9) Push the 75 ohm UNBAL INPUT IMPEDANCE switch.
(10) Adjust the screwdriver adjustment (just to the right of the 0 dBm LEVEL CAL switch) for a meter reading of 0 dBm on the top meter scale. The adjustment of the meter zero should be performed at the same visual angle as the remainder of the tests to reduce parallax error.

(b) Connect the equipment as shown in figure 8-3.

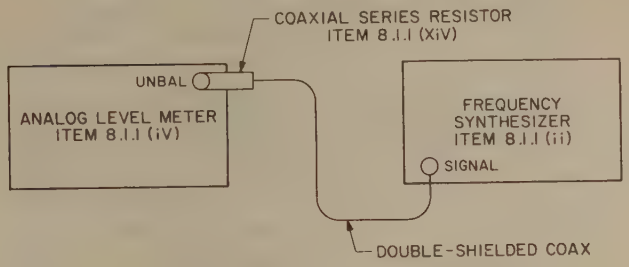


FIGURE 8-3
CALIBRATION OSCILLATOR ADJUSTMENT
HOOKUP DIAGRAM #1

(c) Set the level meter item 8.1.1 (iv) switches and controls as follows:

Switch/Control	Position
0 dBm LEVEL CAL	OFF
METER switch	EXP
INPUT LEVEL (dBm)	−30 (on 10 dB step attenuator) 0 (on 1 dB step attenuator)
INPUT IMPEDANCE	75 ohm UNBAL
HIGH/NORMAL switch	NORMAL

(d) Set the frequency synthesizer item 8.1.1 (ii) switches and controls as follows:

Switch/Control	Position
FREQUENCY	250,000 Hz
AMPLITUDE	−28.3 dBm
FUNCTION	~ (sinewave)

(e) Adjust the frequency synthesizer item 8.1.1 (ii) output signal level using the four MODIFY keys so that the level meter reads exactly −30.0 dBm. Unplug the double shielded coax and coax series resistor from the level meter and connect them to the 6040 BNC input connector. **It is important to use the same double shielded coax and coaxial resistor, in each case, to avoid the replication errors that may result while adjusting the 6040 CAL oscillator level.**

(f) Connect the equipment as shown in figure 8-4.

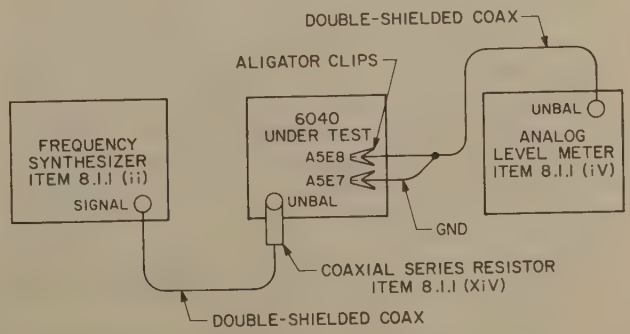


FIGURE 8-4
CALIBRATION OSCILLATOR ADJUSTMENT
HOOKUP DIAGRAM #2

(g) Set the level meter item 8.1.1 (iv) switches and controls as follows:

Switch/Control	Position
0 dBm LEVEL CAL	OFF
METER switch	EXP
INPUT LEVEL (dBm)	+20 (on 10 dB step attenuator) −9 (on 1 dB step attenuator)
INPUT IMPEDANCE	75 ohm UNBAL
HIGH/NORMAL switch	HIGH

(h) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
IMPEDANCE	75 ohm TERM
RANGE dBm	−30 dBm
SELECTIVITY	WIDE
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(i) Adjust the CAL LEVEL potentiometer on the 6040 for a 0 dB meter reading using the level meter item 8.1.1 (iv). The 6040 should read −30.0 ±1.0 dBm. Flip the IMPEDANCE switch on the 6040 to the CAL position. Adjust the internal CAL set potentiometer A14R5 on the 6040 for a 0 dB meter reading on the level meter item 8.1.1 (iv). **Always view the level meter from the same position, because any parallax error will potentially affect the accuracy of the 6040 being adjusted. Additionally, because of the effect of random noise on the meter movement of the level meter in this test, take sufficient time to adjust the meter to the center of the noise variations.**

8.1.17 Initial Filter Balance

(a) Continue this test with the final setup in step 8.1.16 (i).

(b) Flip the 6040 SELECTIVITY switch to the NARROW position. Adjust A4R83 for a 0 dB meter reading on the level meter item 8.1.1 (iv).

8.1.18 1st Mixer Adjustment for Balance

(a) Disconnect the frequency synthesizer and level meter from the 6040. Connect the oscilloscope item 8.1.1 (vi) to either side of A4C38.

(b) Set the 6040 switches and controls as follows:

Switch/Control	Position
RANGE dBm	−30 dBm
IMPEDANCE	50 ohm BRG
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	0.27 kHz
POWER	ON

(c) Adjust A4R15 for a minimum signal level on the oscilloscope screen.

(d) Check for proper mixer balance and noise performance of the unit as follows:

(e) Remove the AC power cord. Operate the unit from battery power. Perform the Unit Calibration test 8.1.23 using WIDE selectivity.

(f) Set the 6040 switches and controls as follows:

Switch/Control	Position
RANGE dBm	−30 dBm
IMPEDANCE	50 ohm BRG
BAL/UNBAL	UNBAL
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	12.00 kHz

(g) Connect the equipment as shown in figure 8-4. Tune the frequency synthesizer 8.1.1 (ii) to 12 kHz at an output level of −30.0 dBm. Place the level meter 8.1.1 (iv) in the 75 ohm high impedance position; set the meter scale to normal.

(h) The 6040 level display should read approximately −30.0 dBm. Note the reading on the level meter 8.1.1 (iv). Remove the coax cable connected to the 6040 BNC input jack. Note the reading on the level meter again; the second reading should be 22 ±1 dB less than the first reading.

(i) Reconnect the coax cable to the 6040 BNC input jack. Change the frequency synthesizer frequency to 180 Hz. Change the SELECTIVITY knob on the 6040 to the NARROW position. Tune the 6040 to 0.18 kHz. Rotate the FINE TUNE knob for a peak level reading (approximately −30.0 dBm). Note the reading on the level meter 8.1.1 (iv). Remove the coax cable connected to the 6040 BNC input jack. Note the reading on the level meter again; the second reading should be 27 ±2 dB less than the first reading. Note that the level meter reading may move erratically around some mean reading; be sure to locate and note the average reading. Reconnect the 6040 AC power cord.

8.1.19 Noise Compensation Wide

WARNING: For units having Serial Nos. 101 to 200 and for the trimpot pairs A24R2 and A24R3 or A24R4 and A24R5, it is possible to configure an adjustment of each odd numbered trimpot fully CCW together with the corresponding even numbered trimpot fully CW to produce a short between +5V and GND. Avoid this situation.

(a) Store the following signals in the frequency synthesizer 8.1.1 (ii).

TABLE 8-4.
BRIDGING INPUT LEVELS

Signal Name	Frequency kHz	Level dBm 50 ohms	Impedance for −30 dBm Level Reading
A	250	−30.04	50 ohms
B	250	−28.30	75 ohms
C	250	−26.16	124 ohms
D	250	−25.80	135 ohms
E	250	−25.36	150 ohms
F	250	−19.71	600 ohms

Note that the Table 8-4 dBm 50 ohm levels take into account bridging error corrections added to the unterminated level readings by the 6040. This will account for observed level differences being greater than those calculated on the basis of the impedance ratio alone.

(b) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	50 ohm BRG
DISPLAY	CENTER PASS BAND
SELECTIVITY	WIDE
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(c) Place trimpots A21R8, A21R40, A24R2, A24R3, A24R4, A24R5 and A24R6 all in their fully CCW positions. Put A24R1 to the center range position.

NOTE: Units with a C-Message equivalent noise response may not have reisistors A24R1, A24R2 and A24R4.

(d) Using a 50 ohm feedthrough 8.1.1 (i) at the unit input, connect the frequency synthesizer 8.1.1 (ii) to the unit. Apply signal A (see Table 8-4). The unit should provide a level reading with an AFC indication on the frequency display.

(e) Adjust the CAL LEVEL control to obtain a −30.0 dBm level reading on the unit.

(f) Reduce the synthesizer signal level by 10 dB and adjust A21R8 to obtain a −40.0 dBm level reading on the unit.

(g) Increase the synthesizer signal level by 10 dB.

(h) Repeat steps (e), (f), and (g) until both −30.0 dBm and −40.0 dBm level readings are obtained without any adjustment. The −40.0 dBm level readings may occasionally show −40.1 dBm or −39.9 dBm but should average −40.0 dBm or lean towards the −40.1 dBm errors.

(i) Place the IMPEDANCE switch in the 600 ohms BRG position. Set the synthesizer to provide an F signal output as per Table 8-4.

(j) Adjust the CAL LEVEL control to obtain a −30.0 dBm level reading on the unit.

(k) Reduce the synthesizer level by 10 dB and adjust A24R6 to obtain a −40.0 dBm level reading.

(l) Increase the synthesizer level by 10 dB.

(m) Repeat steps (j), (k) and (l) until both the −30.0 dBm and the −40.0 dBm level readings are obtained without any further adjustment. Unless restarted, for the remainder of this test the CAL LEVEL control should be set to provide a −30.0 dBm reading for a signal F input from the synthesizer with the IMPEDANCE switch set at 600 ohms.

(n) Set the synthesizer for a signal A output per Table 8-4 and place the unit IMPEDANCE switch in the 50 ohms position. Adjust A24R1 to obtain a −30.0 dBm level reading.

(o) Reduce the synthesizer output level by 10 dB. A −40.0 dBm level reading is desired. If a −40.0 dBm level reading is not obtained, restart the test at step (e) leaving trimpots A24R1 and A24R6 set as they were before the restart.

(p) Place the unit IMPEDANCE switch in the 75 ohms BRG position. Set the synthesizer for a signal B output as shown in Table 8-4.

(q) Note the level readings. Switch the synthesizer output level between a signal B and a signal B −10 dB level. Adjust A24R3 as required to obtain the 10 dB difference between the two level readings.

(r) With the synthesizer providing the signal B output level, adjust A24R2 to obtain a −30.0 dBm level reading.

(s) Reduce the synthesizer output level by 10 dB. A −40.0 dBm level reading is required. If a −40.0 dBm reading is not obtained return to step (q).

(t) Repeat steps (q), (r) and (s) until both the −30.0 dBm and the −40.0 dBm readings are obtained without any further adjustment of A24R2 or A24R3.

(u) With the following test procedure modifications, repeat steps (p) through (t).

75 ohms BRG	to	135 ohms BRG
Signal B	to	Signal D
A24R2	to	A24R4
A24R3	to	A24R5

(v) Verify that, for any of the bridging (BRG) IMPEDANCE switch positions, the corresponding synthesizer input to the unit provides a −30.0 dBm level reading and that a 10 dB reduction in signal level provides a −40.0 dBm level reading.

8.1.20 Noise Compensation, Low Level Correction

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm BRG
DISPLAY	CENTER PASS BAND
SELECTIVITY	WIDE
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(b) Using a 50 ohm feedthrough 8.1.1 (i) at the unit input, connect the synthesizer to the unit and apply a −28.30 dBm 50 ohm signal at a frequency of 250.0 kHz (signal B of Table 8-4).

(c) The unit should show a −30.0 dBm level reading with an AFC frequency mode indication. Place the AFC switch in the OFF position. If the frequency reading changes, tune the unit in such a manner that the AFC ON and AFC OFF frequency readings are identical.

(d) With the AFC switch in the OFF position, lower the synthesizer output by 15 dB to −43.3 dBm. The level reading should be −45.0 dBm ±0.1 dBm.

(e) If the step 20 (d) level reading is more negative than −45.1 dBm, the value of A21R42 should be decreased. If the step 20 (d) level reading is more positive than −44.9 dBm, the value of A21R42 should be increased.

NOTE: In some instances, A21R42 may be found to have been factory replaced by either an open or a short circuit.

For units having Serial Nos. 101 to 200, multipellet diode A21CR4 had a CR1 symbol and was located on switch S3. Resistor A21R42 was soldered between the end of a white/green wire and the junction comprising A21R38, a 4.3 K resistor and A21R41, a 390 ohm resistor.

For units having Serial Nos. 201 and up, diode A21CR4 is located on board A21. When required, resistor A21R42 is mounted on the noncomponent side of A21 along with capacitor A21C30.

(f) Using levels 15 dB below the step 8.1.19 levels shown in the Table 8-4, verify that, for each IMPEDANCE switch position, −45.0 dBm level readings show an accuracy of ±0.1 dBm. If the polarity of the 600 ohm and 50 ohm errors are in opposite directions, a ±0.2 dBm error may be permitted for both the 600 ohm and 50 ohm readings. (NOTE: Leave the RANGE dBm (MAX LEVEL) switch set at −30 dBm)

8.1.21 Noise Compensation for Narrow Bandwidth

NOTE: The Filter Balance Test must have been completed.

(a) Repeat step 8.1.19 (a) if the signals of Table 8-4 have not been retained in storage.

(b) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm BRG
DISPLAY	CENTER PASS BAND
SELECTIVITY	NARROW
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(c) Using a 50 ohm feedthrough 8.1.1 (i) at the unit, connect the frequency synthesizer 8.1.1 (ii) to the unit input. Set the synthesizer for a signal B output.

(d) Adjust the CAL LEVEL control to obtain a −30.0 dBm level reading on the unit.

(e) Reduce the synthesizer signal level by 10 dB and adjust A21R40 to obtain a −40.0 dBm level reading on the unit.

(f) Reduce the synthesizer signal level by an additional 5 dB. The level reading shall be −45.0 ±0.2 dB. A21R40 may be readjusted provided that the −40.0 dBm reading of step (e) is rechecked and verified as being correct.

(g) Using the stored synthesizer signals and by placing the IMPEDANCE switch in each BRG position, verify the −30.0 dBm, −40.0 dBm and −45.0 dBm level readings for each impedance. All −40.0 dBm readings should have an accuracy of ±0.05 dB. All −45.0 dBm readings should have an accuracy of ±0.2 dB.

8.1.22 Excess Noise Check

(a) Remove the 6040 AC power cord for this test. Perform the Unit Calibration test 8.1.23 with the SELECTIVITY switch set on WIDE.

(b) Switch the 6040 IMPEDANCE switch to 50 ohm BRG. Turn the AFC switch OFF. Slowly rotate the TUNE knob from 250 kHz to 12 kHz while watching the LEVEL display. The level reading should remain at −49.9 dBm.

(c) Switch the 6040 SELECTIVITY switch to the NARROW mode. Slowly turn the TUNE knob from 12 kHz to 0.18 kHz while watching the LEVEL display. The level reading should remain at −49.9 dBm. Reconnect the AC power cord to the 6040.

8.1.23 Unit Calibration

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
RANGE dBm	−30 dBm
IMPEDANCE	CAL
SELECTIVITY	As required for measurement
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(b) Verify the presence of an AFC indication and then adjust the CAL LEVEL control to provide a −30.0 dBm level reading on the unit.

8.1.24 Frequency Response

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm TERM
DISPLAY	SIGNAL COUNT
SELECTIVITY	NARROW
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz
Power Source	Battery (remove AC cord)

(b) Set the frequency synthesizer 8.1.1 (ii) for about a −28.0 dBm level with the frequency set at 250.00 kHz. Connect the synthesizer through a double shielded cable via a coaxial series resistor of 27 ohm 8.1.1 (xiv) to the 75 ohm terminated unbalanced input of the analog level meter 8.1.1 (iv). Operate the analog level meter in the 75 ohm unbalanced terminated mode.

NOTE: If a synthesizer having a 75 ohm source impedance is used or, if a 50 ohm to 75 ohm pad is available for transforming a 50 ohm source to a 75 ohm source, then the 27 ohm coaxial series resistor should not be used.

(c) Adjust the synthesizer output level to obtain a −30.0 dBm 75 ohm level reading on the analog level meter.

(d) Disconnect the synthesizer and coaxial series resistor from the analog level meter and connect the synthesizer through the double shielded cable and series resistor to the unbalanced input of the unit. For the 250 kHz signal only, adjust the CAL LEVEL control to obtain a −30.0 dBm level reading from the unit.

(e) For all frequencies other than 250 kHz, do not adjust the CAL LEVEL control. Instead, record any error between the level reading of the unit and a −30.0 dBm reading. Acceptable errors are listed in Table 8-5.

(f) Put the BAL/UNBAL switch to the BAL position.

(g) Apply the unbalanced signal to the balanced inputs with the signal going to input jack E1, (upper blue) and signal ground to input jack E2, (lower blue). **DO NOT** readjust the CAL LEVEL control.

(h) Record any error between the level reading of the unit and a −30.0 dBm reading.

(i) Apply the unbalanced signal to the balanced inputs with the signal going to input jack E2 (lower blue) and signal ground to input jack E1 (upper blue).

(j) Record any error between the level reading of the unit and a −30.0 dBm reading.

(k) Record the algebraic sum of the step (h) and step (j) errors, divided by 2. Acceptable errors are listed in Table 8-5.

(l) Return the BAL/UNBAL switch to the UNBAL position.

(m) Reconnect the synthesizer through the double shielded cable and series resistor to the analog level meter.

(n) Set the synthesizer to another frequency listed in Table 8-5 and repeat steps (c) through (m).

TABLE 8-5
FREQUENCY RESPONSE

Freq. kHz	UNBAL		BAL			
	Tol. dB	(e) Error dB	Tol. dB	(h) E1 Error	(j) E2 Error	(k) $\frac{E1+E2}{2}$ Error
0.3	±0.2		±0.4			
1.1	±0.2		±0.3			
12.0	±0.2		±0.3			
100.0	±0.2		±0.3			
250.0	0.0 Set		±0.1			
500.0	±0.2		±0.3			
1000.0	±0.2		±0.3			
1500.0	±0.2		±0.3			
2000.0	±0.2		±0.3			
2500.0	±0.2		±0.3			
3000.0	±0.2		±0.3			
3250.0	±0.2		±0.3			
3500.0	+0.0-0.5		+0.1-0.6			

8.1.25 Attenuator Tracking

(a) Repeat steps 8.1.24 (a) through 8.1.24 (d). The CAL LEVEL control should only be adjusted for the −30.0 dBm level signal.

(b) For each of the various signal levels listed in Table 8-6, first connect the signal to the analog level meter and adjust the synthesizer to the desired level.

(c) For levels above −50 dBm, place the unit attenuator at the corresponding level range. Transfer the signal from the analog level meter to the unit and record any level reading error generated by the unit.

(d) To obtain levels of −60, −70 and −80 dBm, the attenuator item 8.1.1 (xii) will be required. Connect the attenuator between the synthesizer and the coaxial series resistor. Set the attenuator for any convenient attenuation. Adjust the synthesizer output to obtain a −20 dBm analog meter level reading. Increase the attenuation in 10 dB steps and note any errors observed in the attenuator output at levels of −30, −40 and −50 dBm.

(e) Return the attenuator to the −20 dBm output position and reduce the synthesizer output level to obtain a −50 dBm attenuator output to the analog meter. Connect the attenuator output through the coaxial registor item 8.1.1 (xiv) to the unit under test. Increase the attenuation to obtain −60, −70 and −80 dBm signal levels. Record any level reading errors for the unit. Make any necessary corrections for the previously noted external attenuator errors.

(f) Put the BAL/UNBAL switch to the BAL position. Apply the unbalanced signal to the unit with the signal lead going to input jack E2 (lower blue) and signal ground to input jack E1 (upper blue). Record the level reading error generated by the unit.

(g) Record the algebraic sum of step (c) and (e) errors, divided by 2.

(h) Return the BAL/UNBAL switch to the UNBAL position.

(i) Repeat steps (b) through (h) until the errors for all the levels listed on Table 8-6 have been recorded.

TABLE 8-6
ATTENUATOR TRACKING

Range dBm	UNBAL		BAL.		
	Tol. dB	(c) Error (E1)	Tol. dB	(g) Error (E2)	(f) $\frac{E1+E2}{2}$ Error dB
+20	±0.3		±0.4		
+10	±0.3		±0.4		
+0.0	±0.2		±0.3		
−10.0	±0.2		±0.3		
−20.0	±0.2		±0.3		
−30.0	0.0 Set		±0.1		
−40.0	±0.2		±0.3		
−50.0	±0.2		±0.3		
−60.0	±0.2		±0.3		
−70.0	±0.2		±0.3		
−80.0	±0.2		±0.3		

8.1.26 High Level Frequency Response

(a) Repeat test 8.1.24 step (a) through (n) using a +20.0 dBm signal level from the synthesizer with an attenuator setting of +20 dBm on the unit. The I.F. cover must be in place and properly secured. Frequencies and acceptable errors are listed in Table 8-7.

8.1.28 Input Verification

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm BRG
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

TABLE 8-7
HIGH LEVEL FREQUENCY RESPONSE

	UNBAL		BAL			
Freq. kHz	Tol. dB	(e) Error dB	Tol. dB	(h) E1 Error	(j) E2 Error	(d) $\frac{E1+E2}{2}$ Error
0.3	±0.3		±0.5			
12.0	±0.3		±0.4			
250.0	0.0 Set		±0.1			
1000.0	±0.3		±0.4			
3000.0	±0.3		±0.4			
3500.0	+0.1-0.6		+0.2-0.7			

8.1.27 Linearity

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm BRG
AFC	ON
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(b) Using a 50 ohm feedthrough 8.1.1 (i) at the unit input, connect the synthesizer to the unit. Set the synthesizer for a −28.30 dBm level output at 250.00 kHz. Adjust the unit CAL LEVEL control to obtain a −30.0 dBm level reading.

(c) Increase the synthesizer output level by 0.9 dB. Note the error between the level reading and a −29.1 dBm reading. The error shall be no greater than ±0.1 dB.

(d) Decrease the synthesizer output level by 0.4 dB. Note the error between the level reading and a −29.5 dBm reading. The error shall be 0.0 dB.

(e) Decrease the synthesizer output level an additional 0.5 dB back to the −28.30 dBm level. The level reading should read −30.0 dBm with no error.

(f) Decrease the synthesizer level output in 1.0 dB steps. Note the unit level reading errors. Errors should be 0.0 dB down to and including the −37.0 dBm reading. −38.0 dBm and −39.0 dBm readings may have a ±0.1 dB error.

(g) Starting from a −40.0 dBm reading, decrease the synthesizer output level in 2.0 dB steps. Note the unit level reading errors. Errors may be ±0.2 dB for −42.0 dBm and −44.0 dBm readings. Errors may be ±0.3 dB for −46.0 dBm and −48.0 dBm readings.

(h) Decrease the synthesizer output level to −47.30 dBm. Note the unit level reading error from a −49.0 dBm reading. This error should be no greater than ±0.3 dB.

(i) Put the SELECTIVITY switch to the WIDE position and repeat steps (b) through (h). For wide selectivity −48.0 dBm and −49.0 dBm level readings may be permitted a ±0.4 dB error.

(b) Use a coaxial cable terminated with 50 ohm feedthrough 8.1.1 (i) at the meter end to connect the frequency synthesizer 8.1.1 (ii) first to the analog level meter 8.1.1 (iv) and then to the unit.

(c) Use the analog level meter in the 75 ohm high impedance mode to set the synthesizer output level to the level designated by Table 8-8 for the IMPEDANCE position of the unit. Use a signal frequency of 250.00 kHz.

TABLE 8-8
−30 dBm LEVELS

IMPEDANCE	BRG Input Signal Level dBm 75 ohm	TERM Input Signal Level dBm 75 ohm
50 ohm	−31.80	—
75 ohm	−30.07	−30.00
124 ohm	−27.92	−27.82
135 ohm	−27.56	−27.45
150 ohm	−27.12	−26.99
600 ohm	−21.48	−20.97

NOTE: The difference between BRG and TERM input levels called for in Table 8-8, will correspond to the bridging error corrections that are made by the 6040 unit.

(d) Connect the input signal to the unit. For only the 75 ohm BRG IMPEDANCE position, set the CAL LEVEL control to obtain a −30.0 dBm level reading. The unit should be operating with an AFC indication.

(e) For IMPEDANCE positions other than 75 ohm BRG verify that the unit provides a −30.0 dBm level reading. The unit should be operating with an AFC indication.

(f) After noting the unit level reading error, place the IMPEDANCE switch to a new BRG position and return to step (c).

(g) Put the IMPEDANCE switch in one of the TERM positions. Monitor the signal level at the input to the unit with the analog level meter 8.1.1 (iv).

(h) Set the signal to the level designated by Table 8-8 for the particular IMPEDANCE position of the unit. Verify that the unit does provide a −30.0 dBm level reading. The unit should be operating with an AFC indication.

(i) Put the IMPEDANCE switch in a new TERM position and repeat step (h) until the level readings have been verified for all IMPEDANCE TERM positions.

8.1.29 Termination Verification

(a) Put the BAL/UNBAL switch in the UNBAL position.

(b) With an ohmmeter, verify that for each IMPEDANCE TERM switch positions, the resistance measured equals the value designated for the position on Table 8-9 by no more than ±1%.

TABLE 8-9
DC TERMINATION RESISTANCE

IMPEDANCE TERM POSITION	RESISTANCE ±1%
75 ohm	76.1 ohm
124 ohm	127.0 ohm
135 ohm	139.0 ohm
150 ohm	155.0 ohm
600 ohm	682.0 ohm

NOTE: Shunt AC coupled internal loading will reduce signal impedances to a lower value than the Table 8-9 DC resistance values shown above.

(c) With the unit in a 75 ohm unbalanced bridging input configuration, provide a −30.0 dBm 75 ohm signal to the unit from the synthesizer. The signal should be at a 100 kHz frequency. Tune the unit to obtain a level reading.

(d) Verify that a 4.87 K 1% resistor with a 51 pF parallel capacitor, placed in series with the input reduces the unit level reading by between 5 to 6.5 dB.

(e) Repeat steps (c) and (d) with a change in signal frequency to 3.5 MHz.

(f) Change the unit BAL/UNBAL switch to the BAL position.

(g) Apply the unbalanced signal input to input jack E1, (upper blue). Repeat steps (c), (d) and (e).

(h) Place the unit IMPEDANCE switch in the 135 ohm TERM position.

(i) Verify that placing the 4.87 K resistor and capacitor in series with the input jack E1, input reduces unit level reading by between 15 dB to 20 dB.

8.1.30 Selectivity

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
IMPEDANCE	50 ohm BRG
RANGE dBm	0 dBm
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz
DISPLAY	CENTER PASS BAND

(b) Connect the synthesizer item 8.1.1 (ii) through a double-shielded coax via a 50 ohm feedthrough termination item 8.1.1 (i) to the BNC plug on the 6040 unit. Set the synthesizer to 250,000 Hz at a 0 dBm level. Adjust the CAL LEVEL potentiometer on the 6040 for a 0.0 dBm reading on the display.

(c) Tune the synthesizer both high and low and locate the 0.1 dB, 0.5 dB and 3.0 dB attenuation frequencies. Record the frequencies on Table 8-10. The highest reading (0.0 dB) must occur only in the center of the filter passband.

(d) Rotate the RANGE dBm (MAX LEVEL) switch to the −70 dBm position and tune the synthesizer both high and low in frequency until the level display indicates −70.0 dBm. Record the 70.0 dB attenuation frequencies on Table 8-10.

(e) WIDE FILTER SKIRT THRESHOLD CHECK. Tune the synthesizer to 200,000 Hz. Adjust the synthesizer MODIFY KEYS (← or →) so that the 100 Hz digit position is blinking. Push and hold the ↑ key and let the synthesizer tune between 200,000 and 300,000 Hz. Stop and check those frequencies that show signs of spurious level jumps with the exception of frequencies between the two 70 dB attenuation frequencies recorded for the wide filter on Table 8-10. No spurious frequency should cause a displayed level to exceed −70.0 dBm.

(f) Return the 6040 RANGE dBm (MAX LEVEL) switch to the 0 dBm position. Set the SELECTIVITY switch to the NARROW position. Repeat steps (c) and (d).

(g) NARROW FILTER SKIRT THRESHOLD CHECK. Tune the synthesizer to 246,000 Hz. Adjust the synthesizer MODIFY KEYS (← or →) so that the 10 Hz digit position is blinking. Push and hold the ↑ key and let the synthesizer tune between 246,000 and 254,000 Hz. Stop and check those frequencies that show signs of spurious level jumps with the exception of frequencies between the two 70 dB attenuation frequencies recorded for the narrow filter on Table 8-10. No spurious frequencies should cause a displayed level to exceed −70.0 dBm.

(h) Calculate on Table 8-10 the 0.1 dB, 0.5 dB, 3.0 dB and 70.0 dB bandwidths of the 2 filters and also their center frequencies. The center frequency is the average of the two frequencies producing the 3.0 dB attenuation frequencies.

FILTER ATTENUATION PARAMETER	RECORDED FREQUENCIES AND CALCULATIONS (Hz)		FILTER SELECTIVITY SPECIFICATIONS (Hz)			
			[illegible] FILTER		NARROW FILTER	
	WIDE	NARROW	[illegible]	C-MESSAGE	50 Hz	100 Hz
[illegible] dB Upper ~						
[illegible] dB Lower ~						
[illegible] dB BW (U-L)			1,000 Min.	700 Min.	10 Min.	20 Min.
[illegible] dB Upper ~						
0.5 dB Lower ~						
[illegible] dB BW (U-L)			[illegible] Min.	[illegible] Min.	[illegible] Min.	[illegible] Min.
3.0 dB Upper ~						
3.0 dB Lower ~						
[illegible] dB BW (U-L)			2,900-3,300	1,800-2,200	45-55	80-120
CENTER ~ [illegible]			249,900-250,100	249,900-250,100	249,997-250,003	249,994-250,006
[illegible] dB Upper ~						
[illegible] dB Lower ~						
[illegible] dB BW (U-L)			2000 Max.	6,200 Max.	365 Max.	580 Max.

~ = Frequency BW = Bandwidth U = Upper L = Lower Min. = Minimum Max. = Maximum

TABLE 8-10 FILTER SELECTIVITY

8.1.31 Image and I.F. Rejection

(a) Perform the Unit Calibration using the wide filter selectivity as described in test 8.1.23.

(b) Connect the frequency synthesizer item 8.1.1 (ii) to the 6040 BNC input connector J3, using a double shielded coax cable and a 50 ohm feedthrough termination item 8.1.1 (i).

(c) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
IMPEDANCE	50 ohm BRG
RANGE dBm	AUTO RANGE
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
DISPLAY	CENTER PASS BAND
FREQUENCY (TUNE)	250.00 kHz

(d) Set the frequency synthesizer to 455,000 Hz at a level of 0 dBm. Wait for the 6040 to auto range to a stable level reading. The level reading should be −70.0 dBm.

(e) Set the frequency synthesizer to 5,000,000 Hz at a level of 0 dBm. Wait for the 6040 to auto range to a stable level reading. The level reading should be −70.0 dBm.

(f) Set the Frequency Synthesizer to 10,250,000 Hz at a level of 0 dBm. Wait for the 6040 to auto range to a stable level reading. The level reading should be −70.0 dBm.

8.1.32 2nd and 3rd Harmonic Test

(a) Perform the Unit Calibration using the wide filter selectivity as described in test 8.1.23.

(b) Connect the equipment as shown in figure 8-5.

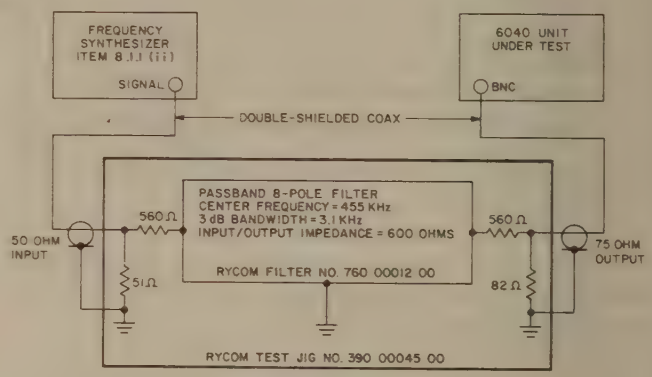


FIGURE 8-5
HARMONIC TEST HOOKUP DIAGRAM

NOTE: Use of a properly constructed filter test jig for this measurement is mandatory for accurate results. The constructional features of the 390 00045 00 test jig shown in figure 8-5 may be obtained on request from Rycom Instruments.

(c) Set the unit switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
IMPEDANCE	75 ohm TERM
RANGE dBm	−20 dBm
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
SIGNAL COUNT	CENTER PASS BAND
FREQUENCY DISPLAY	455.00 kHz

(d) Set the frequency synthesizer to 455,000 Hz at a level of 16.5 dBm. Then use the MODIFY entry keys to change the synthesizer output level until the 6040 LEVEL display reads −20.0 dBm.

(e) Change the RANGE dBm (MAX LEVEL) switch on the 6040 from −20 dBm to −80 dBm. Change the CENTER PASS BAND frequency on the 6040 to 910.00 kHz (2nd Harmonic of 455 kHz). The level reading should be ≤ −90.0 dBm.

(f) Change the CENTER PASS BAND frequency on the 6040 to 1365.00 kHz (3rd Harmonic of 455 kHz). The level reading should be ≤ −90.0 dBm.

8.1.33 Auto Range, Signal Count and 1 Hz Verification

(a) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	AUTO RANGE
IMPEDANCE	50 ohm BRG
FREQUENCY DISPLAY	SIGNAL COUNT
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	250.00 kHz

(b) Using a 50 ohm feedthrough 8.1.1 (i) at the 6040 input, connect the synthesizer in cascade with the attenuator 8.1.1 (xii) to the unit. Set the synthesizer and attenuator for a −32.04 dBm level input to the unit at 250 kHz.

(c) Change the unit input level in 10 dB steps. Proceed through levels −82.04 dBm to +17.96 dBm. Verify that the auto ranging system tracks the signal level through the full level range and provides stable level readings without either of the two ADJUST RANGE indicators flashing.

(d) Change the synthesizer frequency in 100 Hz steps. Verify that the frequency display tracks the synthesizer frequency and provides a SIGNAL COUNT indication.

(e) Put the FREQUENCY DISPLAY switch in the 1 Hz position. Verify that the FREQUENCY DISPLAY does provide 1 Hz resolution. The FREQUENCY DISPLAY should agree with the synthesizer frequency. If a discrepancy is observed, an accurate counter should be used to verify the unit frequency reading.

8.1.34 Final AFC Check

(a) Calibrate the unit per Test 8.1.23 with NARROW selectivity.

(b) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−30 dBm
IMPEDANCE	75 ohm BRG
FREQUENCY DISPLAY	CENTER PASS BAND
SELECTIVITY	NARROW
METER REF	IN
AFC	OFF
RANGE kHz	0.3-650 kHz
FREQUENCY (TUNE)	300 Hz

(c) Using a 50 ohm feedthrough 8.1.1 (i) at the unit input, connect the synthesizer to the unit. Set the synthesizer for a −38.3 dBm 50 ohm output level and a 300 Hz frequency.

(d) Tune the unit to obtain a level reading between −44.0 dBm and −46.0 dBm, at a frequency below 300 Hz. Put the AFC switch in the ON position. The unit should auto tune to 300 Hz and display an AFC indication.

(e) Return the AFC switch to the OFF position. Tune the unit to obtain a level reading between −44.0 dBm and −46.0 dBm at a frequency above 300 Hz. Put the AFC switch in the ON position. The unit should auto tune to 300 Hz and display an AFC indication.

(f) Put the unit SELECTIVITY switch to the WIDE position. Set the synthesizer frequency to 10 kHz.

(g) Put the AFC switch to the OFF position. Tune the unit to obtain a −44.0 to −46.0 dBm level reading at a frequency just below the signal frequency. Put the AFC switch to the ON position. The unit should auto tune to the signal frequency and display an AFC indication.

(h) Put the AFC switch to the OFF position. Tune the unit to obtain a −44.0 to −46.0 dBm level reading at a frequency just above the signal frequency. Put the AFC switch to the ON position. The unit should auto tune to the signal frequency and display an AFC indication.

(i) Put the SELECTIVITY switch to the NARROW position. The AFC indication and frequency display should not be disturbed. Return the SELECTIVITY switch to the WIDE position.

(j) Change the RANGE kHz to 550-1650 and set the synthesizer frequency to 1650 kHz. Repeat steps (g), (h) and (i).

(k) Change the RANGE kHz to 1300-2400 and set the synthesizer frequency to 1300 kHz. Repeat steps (g), (h) and (i).

(l) Set the sythesizer frequency to 2400 kHz. Repeat steps (g), (h) and (i).

(m) Change the RANGE kHz to 2000-3500 and set the synthesizer frequency to 2000 kHz. Repeat steps (g), (h) and (i).

(n) Set the synthesizer frequency to 3500 kHz. Repeat steps (g), (h) and (i).

8.1.35 Low Bat and Bat Test

(a) Remove the AC power cord from the unit.

(b) Set the POWER switch to OFF.

(c) Remove the battery from the unit.

(d) Set the external DC power supply 8.1.1 (viii) for a 12.0 V DC output. Monitor the supply voltage with digital VOM 8.1.1 (v).

(e) Connect the positive lead of the DC power supply to A1E1 and the negative lead to chassis ground.

(f) Turn the unit POWER switch to ON and calibrate the unit using the wide filter selectivity per test 8.1.23 Unit Calibration.

(g) With the DEMODULATOR control full clockwise and with a 1.0 kHz SSB tone, observe and record the power supply current. The current should be less than 400 mA.

(h) While using the calibration oscillator as a signal source, reduce the DC supply voltage. Note the DC voltage at which the unit level reading varies substantially with the supply voltage. This supply voltage should be between 11.4 and 11.7 volts.

(i) Vary the DC power supply and adjust A22R3 until the LOW BAT indicator, located in the LCD LEVEL DISPLAY starts to flash at 11.8 volts. The DC voltage must be changed slowly; the transient that results from an abrupt reduction in the supply voltage is coupled through A22C3 and may trigger a premature flashing signal.

(j) Verify that the unit will operate in the LOW BAT mode for only 25 minutes prior to complete equipment turn off.

(k) Verify that placing the POWER switch to the CHARGE position resets the 25 minute shut down period.

(l) Adjust A21R46 to provide a meter reading at the bottom edge of the BAT OK area when the DC supply voltage is 11.8 volts.

NOTE: Units having Serial Nos. 101-200, omitted A21R46. A21R34 was selected to provide the desired meter reading.

8.1.36 Out of Range Indicators and Meter Check

(a) Calibrate the unit per Test 8.1.23 Unit Calibration for wide selectivity.

(b) Adjust the CAL LEVEL control and verify that for the −30 dBm RANGE dBm, level readings above −29.1 dBm blank the LEVEL dBm display and provide an above range indication. Return the CAL LEVEL control to the −30.0 dBm level reading position.

(c) With the METER REF knob in the IN position, verify a meter reading at the top of the meter scale for a −30.0 dBm level reading with a −30 dBm RANGE dBm (MAX LEVEL) switch setting.

(d) Put the RANGE dBm (MAX LEVEL) to the −20 dBm range. Verify a mid-range meter reading for a −30.0 dBm level reading.

(e) Using the CAL LEVEL control, verify that the below-range-indicator starts flashing as the level reading drops below −30.0 dBm. Return the CAL LEVEL control to the −30.0 dBm level reading position.

(f) Place the RANGE dBm (MAX LEVEL) switch in the −10 dBm range. Verify a bottom of the scale meter reading.

(g) Put the RANGE dBm (MAX LEVEL) switch to the −20 dBm range. Pull out the METER REF knob. Verify the meter reading can be set to mid-range with the METER REF control.

(h) With the CAL LEVEL control, set the LEVEL dBm display for a −29.0 dBm level reading. Verify that the meter reads approximately 75% full scale.

(i) With the CAL LEVEL control, set the LEVEL dBm display for a −31.0 dBm level reading. Verify that the meter reads approximately 25% full scale.

8.1.37 SSB Oscillator Frequency Check

(a) Using a 10:1 probe 8.1.1 (xi) connect the frequency counter 8.1.1 (iii) to the cathode of A5CR2.

(b) Put the DEMODULATOR switch in the LSB position. The counter should indicate a 453,500 Hz ±20 Hz frequency.

(c) Put the DEMODULATOR switch in the USB position. The counter should indicate a 456,500 Hz ±20 Hz frequency.

8.1.38 Audio Signal-To-Noise and Audio Level

(a) Calibrate the unit per Test 8.1.23 Unit Calibration, with NARROW selectivity.

(b) Use analog level meter 8.1.1 (iv) in the 600 ohm balanced, high impedance mode. Monitor the signal level across the unit speaker.

(c) With the DEMODULATOR switch in the LSB position and with the LEVEL (audio) control fully clockwise, verify a greater than +10 dBm 600 ohm level across the speaker.

(d) Repeat step (c), for the USB position of the DEMODULATOR switch.

(e) Adjust the LEVEL (audio) control to obtain a 0.0 dBm 600 ohm level across the speaker.

(f) Place the IMPEDANCE switch to the 50 ohm BRG position. The signal level across the speaker should now be less than −25 dBm.

(g) Place the SELECTIVITY switch to the WIDE position. The signal level across the speaker should be less than −20 dBm.

8.1.39 AM Monitoring

(a) No external connections are required.

(b) Set the instrument switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
RANGE dBm	−80 dBm
IMPEDANCE	75 ohm BRG
SELECTIVITY	WIDE
AFC	OFF
DEMODULATOR switch	AM
RANGE kHz	550-1650 kHz
LEVEL (audio)	Mid Range

(c) Touch the UNBAL input with a short antenna such as a 2 inch clip lead. Tune to any local AM radio station and verify that AM monitoring is performed by the unit. The RANGE dBm (MAX LEVEL) adjustment will be required for good audio quality. Check for reasonable fidelity.

(d) Plug a headset having an impedance of 100 ohm to 1 K ohm into the OUTPUT jack and verify the external audio output operation.

8.1.40 Frequency Limit Checks

(a) Set the SELECTIVITY switch to NARROW and the AFC switch to OFF.

(b) Slowly tune down the frequency and note the frequency at which the display shows all zero's. This frequency should be between 160 and 190 Hz.

(c) Continue to tune down in frequency and verify that the display remains at an all zero condition.

8.1.41 Cal Level Control Centering

(a) Calibrate the unit per test 8.1.23 Unit Calibration, using the WIDE selectivity.

(b) Set the CAL LEVEL potentiometer to mid-range by measuring the voltage on the center pin (wiper) of the potentiometer and setting it to 5.00 V DC. Adjust A4R108 for a −30.0 dBm reading on the 6040 level display.

8.1.42 Final Filter Balance

(a) Operate the unit at an ambient temperature between 20°C to 25°C for at least 4 hours, preferably 8 hours. Use a dummy case with an access hole located in line with trimpot A4R83. This dummy case is necessary in order to avoid disturbing the equilibrium of the internal thermal environment achieved by operating the unit for 8 hours prior to adjustment.

(b) Calibrate the unit per test 8.1.23, Unit Calibration, using WIDE selectivity.

(c) Put the SELECTIVITY switch to the NARROW position and using the access hole in the rear of the case, adjust A4R83 such that WIDE and NARROW level readings are identical.

8.1.43 Noise Power Ratio

(a) Perform the Unit Calibration using the wide filter selectivity as described in Test 8.1.23, Unit Calibration.

(b) Hook up the noise generator 8.1.1 (x) to the 6040 INPUT BNC with a double-shielded coax cable.

(c) Set the 6040 switches and controls as follows:

Switch/Control	Position
BAL/UNBAL	UNBAL
IMPEDANCE	75 ohm TERM.
RANGE dBm	−30 dBm
SELECTIVITY	WIDE
AFC	OFF
RANGE kHz	550-1650 kHz
DISPLAY Switch	CENTER PASS BAND
FREQUENCY Display	1002.00 kHz

(d) Set up the Marconi Noise Generator 8.1.1 (x) as follows:

Switch/Control	Position
NOISE Switch	ON (Center position)
ATTENUATOR	−2 dBm
LOWPASS FILTERS	3284 kHz ⟶ IN
	Others ⟶ OUT
BAND REJECT FILTERS	ALL ⟶ OUT
METER CAL	0 dBm (Rotate Noise Level Knob)

(e) Adjust the noise generator for a −30.0 dBm reading on the 6040. Use the noise generator attenuator to adjust for steps greater than ±1 dB. Use the Noise Level Control to adjust levels less than ±1 dB. There will be noise jitter on the 6040 level display readout; take the average −30.0 dBm reading.

(f) Switch the 1002 kHz band reject filter on the Noise Generator to the → IN position. Change the RANGE dBm (MAX LEVEL) switch on the 6040 to −70 dBm. The level shown on the 6040 must be ≤−87.0 dBm.

8.2 NOTES ON TROUBLE SHOOTING THE 6040 SELECTIVE LEVEL METER

A Gain Distribution Diagram figure 8-6 and a board location diagram figure 8-7 has been provided at the end of this chapter as an aid for trouble shooting. Bias voltages, signal frequencies and waveshape information may be found in the chapter 12 schematic diagrams. Figure 6-5 should be consulted to verify frequency counter control signal timing. Chapter 10 contains figures showing the component layout for each circuit board. Chapter 11 shows the mechanical and electrical functions of the analog and digital integrated circuits used in the 6040. The unit calibration oscillator will provide an adequate input test signal for trouble shooting most problems.

8.2.1 Fuses

The 6040 contains both line and battery protection fuses. These are located on the power supply assembly A15 and on the power supply circuit card A1. When replacing the 2 Amp battery protection fuse on the A1 board, disconnect one of the battery leads. This will prevent the accidental shorting of the battery and associated circuitry by screwdrivers or other tools.

8.2.2 Input Selector (A2), Attenuator/Summing Amplifier (A3), and I.F. (A4) Circuit Board Problems.

The simplest method for trouble shooting the Input Selector, Attenuator/Summing Amplifier and I.F. circuits, is to inject a test signal into the 6040 input circuitry and to locate the problem area by measuring the various circuit stage signal voltage levels. Inject the calibration oscillator test signal by positioning the IMPEDANCE switch in the CAL mode. Tune the 6040 to 250.00 kHz, with WIDE selectivity and the AFC turned ON. Measure the signal voltages with a high-input-impedance AC voltmeter which has a flat frequency response out to 5 MHz and 100 micro volt sensitivity. The nominal signal voltage levels for each stage are shown in the Gain Distribution Diagram figure 8-6. For those stages after the second I.F. mixer, set the RANGE dBm (MAX LEVEL) switch in the −30 dBm position and compare the measured signal voltages to those shown in figure 8-6. For those stages before the second I.F. mixer, set the RANGE dBm (MAX LEVEL) switch in the −70 dBm position and compare the measured signal voltages to those shown in figure 8-6 multiplied by 100.

8.2.3 Frequency Display Problems

Check the frequency of the signal at A8I27C-10. While operating the unit in the AFC mode this frequency should be ½ the input frequency. When the unit is not in an AFC mode this frequency will be the pass band frequency plus 5.0 kHz. If the A8I27C-10 frequency is incorrect, the problem is in the count signal generation circuitry. In this event, input signals to A8 from the local oscillators and from the second I.F. and frequency subtraction frequencies should be checked.

If the A8I27C-10 signal has the correct frequency, then the frequency counter control signals should be checked. The timing diagram for these signals is shown in figure 6-5.

8.2.4 Level Display Problems

If level displays are obtained but the level readings are incorrect, then the adjustment procedures for A21 and A24 need to be performed (8.1.12, 8.1.19, 8.1.20 and 8.1.21).

If the problem involves more than an observed reading error, check the response of the analog meter. If the meter responds to the CAL LEVEL control or unit tuning the problem lies in the digital circuitry that generates the level display. If there is no meter response, check for a 43.46 Hz square wave at the cathode of A21CR1. If the square wave is present, check the I.F. input, the level detector and log pulse generator portions of A21. Refer to chapter 7 for an explanation of the level display system operation.

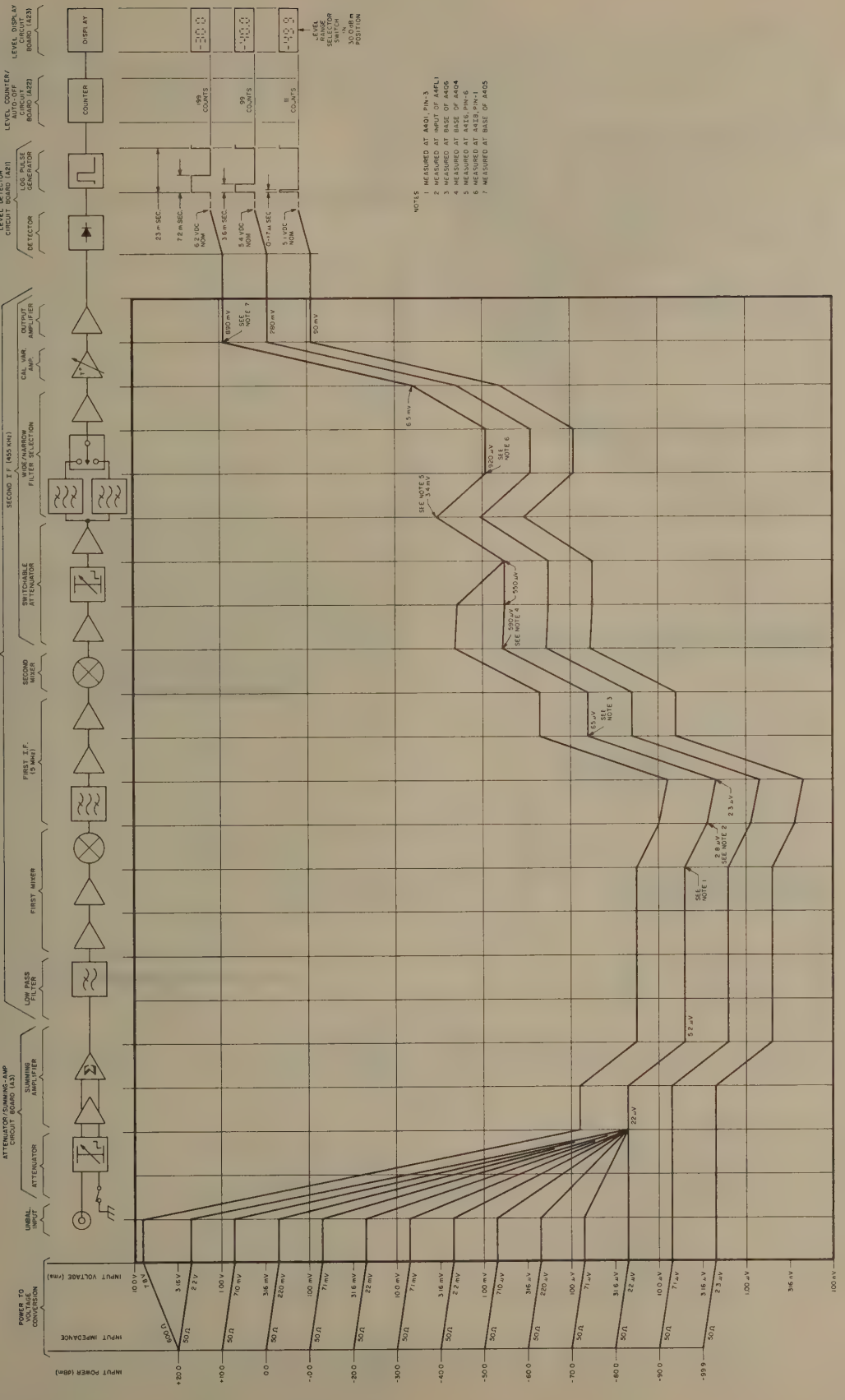
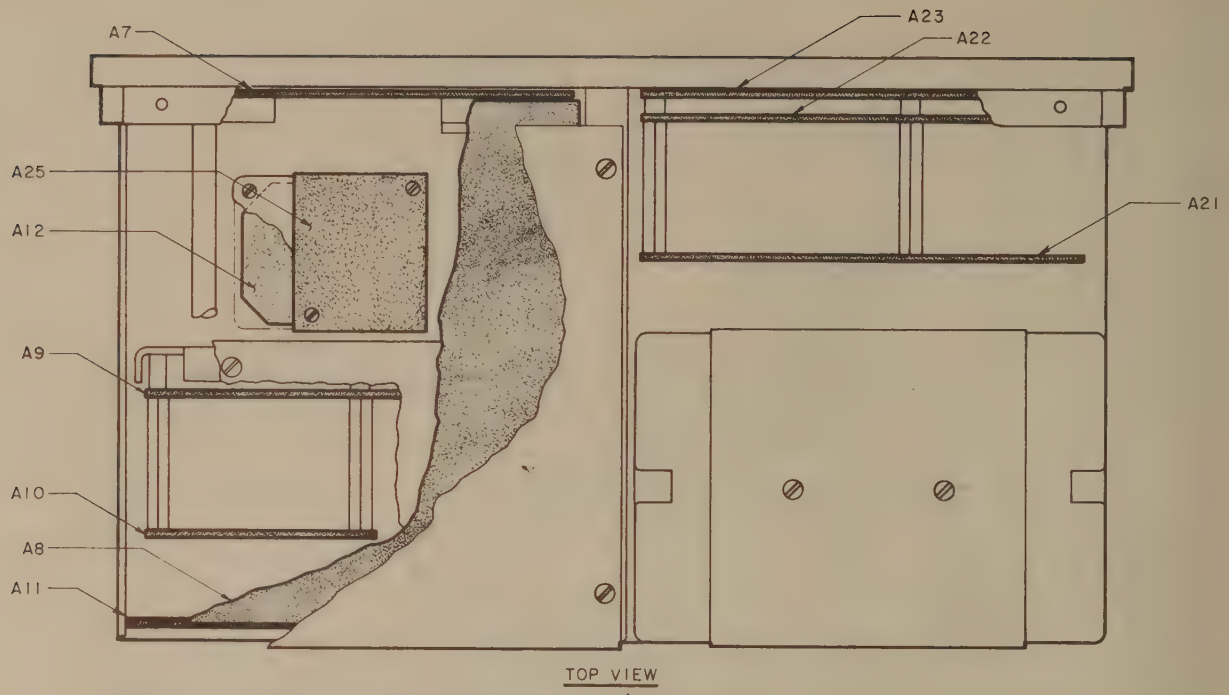
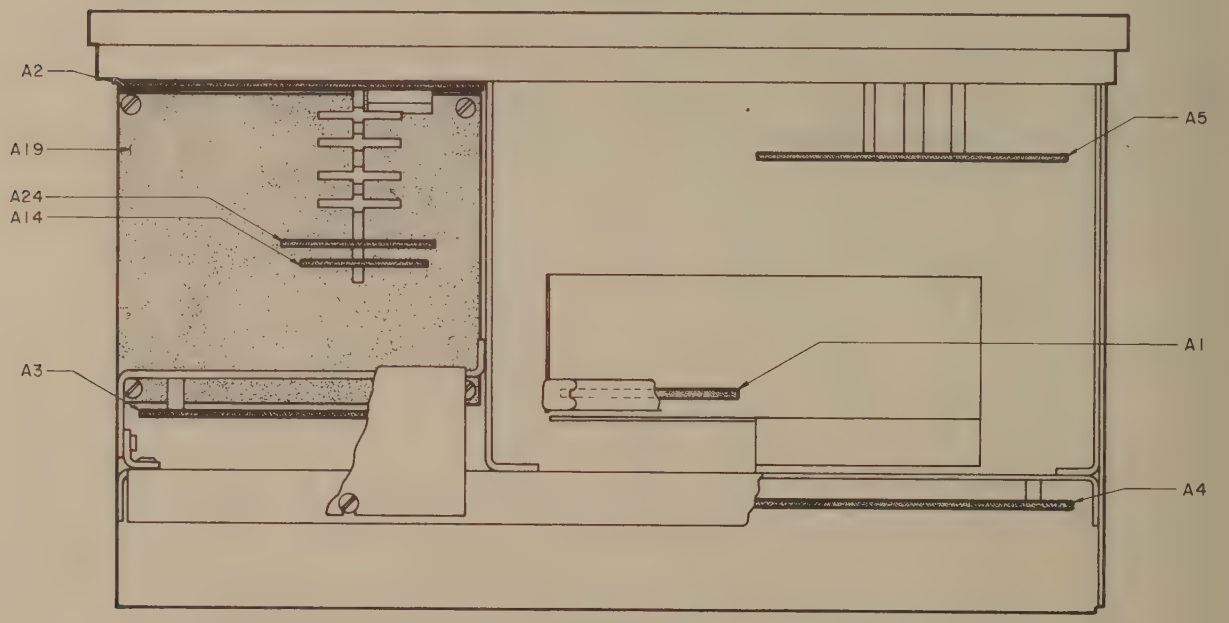


FIGURE 8-6
6040 GAIN DISTRIBUTION DIAGRAM



TOP VIEW



BOTTOM VIEW

A1 - POWER SUPPLY
A2 - INPUT SELECTOR
A3 - ATTENUATION/SUMMING AMP.
A4 - I.F.
A5 - MONITOR
A7 - FREQUENCY DISPLAY
A8 - TIMING & COUNTER INPUT
A9 - 1st L.O.
A10 - 1st L.O. BUFFER/AMP.
A11 - PHASE LOCK LOOPS
A12 - 2nd L.O.
A14 - CALIBRATION OSC.
A19 - AUTO RANGING
A21 - LEVEL DETECTOR
A22 - LEVEL DISPLAY
A24 - NOISE COMPENSATION
A25 - AFC LOW PASS FILTER

FIGURE 8-7
6040 PRINTED WIRING BOARD LOCATION

CHAPTER 9
PARTS LIST

9.0 HOW TO ORDER PARTS

When ordering parts, always include:

a. Name, Model and Serial Number of the instrument.
b. Module and reference designation.
c. Part number.
d. Description.

Order parts from:

RYCOM INSTRUMENTS INC.
9351 East 59th Street
Raytown, Missouri 64133 Telephone 816-353-2100

PARTS LIST

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
	PARTS LOCATED ON FRONT PANEL OR CHASSIS		
BT1	Battery, 12 V, rechargeable	770 00010 02	1
C1	Cap, Feed-thru, 0.001 μF	680 00003 00	4
C2	Cap, Feed-thru, 0.001 μF, same as C1		
C3	Cap, Feed-thru, 0.001 μF, same as C1		
C4	Cap, Feed-thru, 0.001 μF, same as C1		
C5	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	1
CR1	Diode, Stabistor, 1N5179 Serial Nos. 101-200 only	410 00041 00	1
E1	Banana Jack, Blue	812 00083 06	2
E2	Banana Jack, Blue, same as E1		
E3	Banana Jack, Black	812 00083 00	1
J1	Connector, electrical, power	812 00066 00	1
J2	Jack, phone	812 00009 00	1
J3	BNC receptacle	812 00079 00	1
J4	BNC receptacle	812 00076 00	1
J5	Connector edge card 20-pin	812 00011 01	1
J6	Connector Assy	120 00203 00	1
J7	Jack, tip	812 00085 00	1
J8	Connector Assy	120 00202 00	1
LS1	Loudspeaker, 3 inch	743 00003 00	1
M1	Meter W/Vertical Scale	740 00014 00	1
R1	Res, Var, 10 k ohms W/push-pull switch S1	542 00022 00	1
R2	Res, Var, 2500 ohms ±30%, 1/2 W, comp	540 00001 03	1
R3	Res, Var, 10 k ohms ±30%, 1/2 W, comp	540 00001 10	1
R4	Res, Var, 25 k ohms ±30%, 1/3 W, comp	540 00001 15	1
S1	Switch, part of R1		
S2	Switch, Rotary	720 00059 00	1
S3	Switch, Rotary	720 00063 00	1
S4	Switch, Toggle	722 00015 00	1
S5	Switch, Toggle	722 00015 03	1
	POWER SUPPLY ASSEMBLY A1		
A1	Circuit Card Assembly, Power Supply Serial Nos. 101-200 only	110 00150 00	1
A1	Circuit Card Assembly, Power Supply Serial Nos. 201 up	110 00150 01	1
A1C1	Cap, 1000 μF (+50, −10%), 35 wvdc, elect'c	630 00007 06	1
A1C2	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	4
A1C3	Cap, 0.1 μF, same as A1C2		
A1C4	Cap, 0.1 μF, same as A1C2		
A1C5	Cap, 0.1 μF, same as A1C2		
A1CR1	Diode, Rectifier, type CB80	410 00023 00	1
A1F1	Fuse, 2 Amp, type AGA2	723 00002 00	1
A1I1	IC, 5 V regulator, type LM340T-5.0	431 00064 01	1
A1I2	IC, 10 V regulator, type LM340T-10.0	431 00072 01	2
A1I3	IC, type LM340T-10.0, same as A1I2		

PARTS LIST

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A1Q1	Transistor, PNP, type 2N3702	400 00012 00	1
A1Q2	Transistor, NPN, type 2N3704	400 00013 00	1
A1R1	Res, 210 ohms ±5%, 1/4 W, 70°C, film	561 00004 04	1
A1R2	Res, var. 500 ohms ±20%, 1/2 W, cermet	542 00003 00	1
A1R3	Res, 75 ohms ±5%, 1/4 W, carbon Serial Nos. 101-200 only	500 00750 00	1
A1R4	Res, 15 k ohms ±5%, 1/4 W, carbon	500 00153 00	1
A1R5	Res, 2200 ohms ±5%, 1/4 W, carbon Serial Nos. 101-200 only	500 00222 00	1
A1R5	Res, 1800 ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00182 00	1
A1R6	Res, 510 ohms ±5%, 1/4 W, carbon Serial Nos. 101-200 only	500 00511 00	1
A1R6	Res, 2000 ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00202 00	1
A1R7	Res, 340 ohms ±2%, 1/2 W, 70°C, film Serial Nos. 101-200 only	561 00003 02	1
A1R7	Res, 412 ohms ±2%, 1/2 W, 70°C, film Serial Nos. 201 up	561 00003 01	1
A1R8	Res, 2.0 ohms ±5%, 3 W, wire wound	560 00001 05	1
A1R9	Res, 100 ohms ±5%, 1/4 W, carbon Serial Nos. 101-200 only	500 00101 00	1
A1R9	Res, 430 ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00431 00	1
A1R10	Res, 1.0 ohm ±10%, 5 W, power WW	560 00008 00	1
	INPUT SELECTOR ASSEMBLY A2		
A2	Circuit Card Assembly, Input Selector	110 00136 00	1
A2C1	Cap, 10 μF ±20%, 200 wvdc, mylar	620 00023 01	1
A2C2	Cap, 2 μF ±10%, 200 wvdc, mylar	620 00023 02	2
A2C3	Cap, 2 μF, same as A2C2		
A2C4	Cap, 0.47 μF ±20%, 200 wvdc, mylar	620 00025 04	1
A2J1	Jack, phono, printed circuit	812 00059 00	2
A2J2	Jack, phono, same as A2J1		
A2J3	Conn Assy, rect 8-pin	813 00021 08	1
A2R1	Res, 8870 ohms ±1%, 1/8 W, metal film	511 28871 00	2
A2R2	Res, 129 ohms ±0.1%, 1 W, metal film 25ppm	513 01290 50	1
A2R3	Res, 8870 ohms, same as A2R1		
A2R4	Res, 76.8 ohms ±0.1%, 1 W, metal film 25ppm	513 07688 50	1
A2R5	Res, 60.4 k ohms ±1%, 1/8 W, metal film	511 26042 00	1
A2R6	Res, 690 ohms ±0.1%, 1 W, metal film 25ppm	513 06900 50	1
A2R7	Res, 17.8 k ohms ±1%, 1/8 W, metal film	511 21782 00	1
A2R8	Res, 156 ohms ±0.1%, 1 W, metal film 25ppm	513 01560 50	1
A2R9	Res, 15.8 k ohms ±1%, 1/8 W, metal film	511 21582 00	1
A2R10	Res, 140 ohms ±0.1%, 1 W, metal film 25ppm	513 01400 50	1
A2R11	Res, 10 k ohms ±5%, 1/4 W, carbon film	500 00103 00	1
A2S1	Switch, toggle, 3PDT	722 00014 00	1
A2S2	Switch, rotary 12-position	720 00066 00	1
A2S3	Switch, rotary 12-position	720 00060 00	1
	ATTENUATOR/SUMMING AMP ASSEMBLY A3		
A3	Circuit Card Assembly, Attenuator/Summing Amp	110 00137 00	1
A3C1	Cap, 39 μF ±10%, 10 wvdc, tantalum	640 00004 00	2
A3C2	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	9
A3C3	Cap, 10 μF, same as A3C2		
A3C4	Cap, 10 μF, same as A3C2		
A3C5	Cap, 10 μF, same as A3C2		
A3C6	Cap, 10 pF ±5%, 100 wvdc silver mica	610 20010 21	1
A3C7	Cap, 5 pF ±5%, 100 wvdc silver mica	610 20005 21	1
A3C8	Cap, 10 μF, same as A3C2		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A3C9	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	4
A3C10	Cap, 10 μF, same as A3C2		
A3C11	Cap, 10 μF, same as A3C2		
A3C12	Cap, 10 μF, same as A3C2		
A3C13	Cap, 39 μF, same as A3C1		
A3C14	Cap, 10 μF, same as A3C2		
A3C15	Cap, var, 5.5-18 pF, ceramic	660 00004 00	1
A3C16	Cap, 1 pF ±5%, NPO, ceramic	601 00001 36	2
A3C17	Cap, 5 pF ±5%, NPO, ceramic	601 00001 38	1
A3C18	Cap, 1 pF, same as A3C16		
A3C19	Cap, 3.9 pF ±5%, NPO, ceramic	601 00001 37	1
A3C20	Cap, 0.1 μF, same as A3C9		
A3C21	Cap, 0.1 μF, same as A3C9		
A3C22	Cap, 0.1 μF, same as A3C9		
A3I1	Integrated Circuit, TO-92 LM340LAZ-10	431 00060 00	1
A3K1	Relay, Latching 2A2B	705 00004 00	4
A3K2	Relay, Latching, same as A3K1		
A3K3	Relay, Latching, same as A3K1		
A3K4	Relay, Latching, same as A3K1		
A3L1	Parasitic Suppressor	701 00057 00	1
A3Q1	Transistor, PNP, type MPQ3799	400 00047 00	1
A3Q2	Transistor, NPN, type MPSA18, MOT.	400 00037 01	1
A3Q3	Transistor, PNP, type 2N5087, Fairchild	400 00021 02	1
A3R1	Res, 4930 ohms ±0.1%, 1/2 W, MF, 25ppm	513 04931 30	4
A3R2	Res, 50.5 ohms ±0.1%, 1/2 W, MF, 25ppm	513 05058 30	4
A3R3	Res, 4930 ohms, same as A3R1		
A3R4	Res, 50.5 ohms, same as A3R2		
A3R5	Res, 4480 ohms ±0.1%, 1/2 W, MF, 25ppm	513 04481 30	2
A3R6	Res, 556 ohms ±0.1%, 1/2 W, MF, 25ppm	513 05560 30	2
A3R7	Res, 3400 ohms ±0.1%, 1/2 W, MF, 25ppm	513 03401 30	2
A3R8	Res, 2320 ohms ±0.1%, 1/2 W, MF, 25ppm	513 02321 30	2
A3R9	Res, 4930 ohms, same as A3R1		
A3R10	Res, 50.5 ohms, same as A3R2		
A3R11	Res, 4930 ohms, same as A3R1		
A3R12	Res, 50.5 ohms, same as A3R2		
A3R13	Res, 4480 ohms, same as A3R5		
A3R14	Res, 556 ohms, same as A3R6		
A3R15	Res, 3400 ohms, same as A3R7		
A3R16	Res, 2320 ohms, same as A3R8		
A3R17	Res, 9880 ohms ±0.1%, 1/2 W, MF, 50ppm	513 09881 00	2
A3R18	Res, 1200 ohms ±5%, 1/2 W, carbon film	502 00122 00	2
A3R19	Res, 324 ohms ±1%, 1/8 W, metal film	511 23240 00	4
A3R20	Res, 324 ohms, same as A3R19		
A3R21	Res, 4990 ohms ±1%, 1/8 W, metal film	511 24991 00	2
A3R22	Res, 2550 ohms ±1%, 1/8 W, metal film	511 22551 00	1
A3R23	Res, 4120 ohms ±1%, 1/8 W, metal film	511 24121 00	1
A3R24	Res, 3400 ohms ±1%, 1/8 W, metal film	511 23401 00	1
A3R25	Res, 10.1 k ohms ±0.1%, 1/2 W, MF, 50ppm	513 01012 00	2
A3R26	Res, 210 ohms ±1%, 1/8 W, metal film	511 22100 00	1
A3R27	Res, 324 ohms, same as A3R19		
A3R28	Res, 324 ohms, same as A3R19		
A3R29	Res, 4990 ohms, same as A3R21		
A3R30	Res, 732 ohms ±1%, 1/8 W, metal film	511 27320 00	1
A3R31	Res, 2370 ohms ±1%, 1/8 W, metal film	511 22371 00	1
A3R32	Res, 1910 ohms ±1%, 1/8 W, metal film	511 21911 00	1
A3R33	Res, 10.1 k ohms, same as A3R25		
A3R34	Res, 9880 ohms, same as A3R17		
A3R35	Res, 1200 ohms, same as A3R18		
A3R36	Res, 120 ohms ±5%, 1/4 W, carbon film	500 00121 00	1

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A3W1/P1	Cable Assembly, Coax	152 05057 00	1
A3W2/P2	Cable Assembly, Coax	152 05058 00	1
A3W3/P3	Cable Assembly, Coax	152 05059 00	1
A3W4/P4	Cable Assembly W/14-pin conn.	151 00020 02	1
	I.F. ASSEMBLY A4		
A4	Circuit Card Assembly, I.F. 50/3100 Hz	110 00138 00	1
A4	Circuit Card Assembly, I.F. 100/3100 Hz	110 00138 01	1
A4	Circuit Card Assembly, I.F. 50/C-Message	110 00138 02	1
A4	Circuit Card Assembly, I.F. 100/C-Message	110 00138 03	1
A4C1	Cap, 300 pF ±5%, 100 wvdc, silver mica	610 20300 21	1
A4C2	Cap, 30 pF ±5%, 100 wvdc, silver mica	610 20030 21	1
A4C3	Cap, 549 pF ±1%, 100 wvdc, silver mica	610 20549 01	1
A4C4	Cap, 168 pF ±1%, 100 wvdc, silver mica	610 20168 01	1
A4C5	Cap, 435 pF ±1%, 100 wvdc, silver mica	610 20435 01	1
A4C6	Cap, 228 pF ±2%, 100 wvdc, silver mica	610 20228 11	1
A4C7	Cap, 470 pF ±5%, 100 wvdc, silver mica	610 20470 21	1
A4C8	Cap, 110 pF ±5%, 100 wvdc, silver mica	610 20110 21	1
A4C9	Cap, 240 pF ±5%, 100 wvdc, silver mica	610 20240 21	1
A4C10	Cap, 210 pF ±1%, 100 wvdc, silver mica	610 20210 01	1
A4C11	Cap, 10 µF ±20%, 15 wvdc, tantalum	640 00001 01	15
A4C12	Cap, 0.1 µF ±10%, 50 wvdc, mono	600 00015 01	36
A4C13	Cap, 10 µF, same as A4C11		
A4C14	Cap, 0.1 µF, same as A4C12		
A4C15	Cap, 0.1 µF, same as A4C12		
A4C16	Cap, 10 µF, same as A4C11		
A4C17	Cap, 0.1 µF, same as A4C12		
A4C18	Cap, 0.1 µF, same as A4C12		
A4C19	Cap, 10 µF, same as A4C11		
A4C20	Cap, 0.1 µF, same as A4C12		
A4C21	Cap, 250 pF ±5%, 100 wvdc, silver mica	610 20250 21	1
A4C22	Cap, 0.1 µF, same as A4C12		
A4C23	Cap, 0.1 µF, same as A4C12		
A4C24	Cap, 0.1 µF, same as A4C12		
A4C25	Cap, 0.1 µF, same as A4C12		
A4C26	Cap, 0.1 µF, same as A4C12		
A4C27	Cap, 0.1 µF, same as A4C12		
A4C28	Cap, 150 pF ±5%, 100 wvdc, silver mica	610 20150 21	1
A4C29	Cap, 0.1 µF, same as A4C12		
A4C30	Cap, 10 µF, same as A4C11		
A4C31	Cap, 0.1 µF, same as A4C12		
A4C32	Cap, 0.1 µF, same as A4C12		
A4C33	Cap, 0.1 µF, same as A4C12		
A4C34	Cap, 600 pF ±5%, 100 wvdc, silver mica	610 20600 21	1
A4C35	Cap, 0.1 µF, same as A4C12		
A4C36	Cap, 10 µF, same as A4C11		
A4C37	Cap, 10 µF, same as A4C11		
A4C38	Cap, 1 µF ±20%, 100 wvdc, mylar	620 00023 00	1
A4C39	Cap, 10 µF, same as A4C11		
A4C40	Cap, 0.1 µF, same as A4C12		
A4C41	Cap, 0.1 µF, same as A4C12		
A4C42	Cap, 0.1 µF, same as A4C12		
A4C43	Cap, 0.1 µF, same as A4C12		
A4C44	Cap, 10 µF, same as A4C11		
A4C45	Cap, 0.1 µF, same as A4C12		
A4C46	Cap, 0.1 µF, same as A4C12		
A4C47	Cap, 10 µF, same as A4C11		
A4C48	Cap, 0.1 µF, same as A4C12		
A4C49	Cap, 10 µF, same as A4C11		
A4C50	Cap, 0.1 µF, same as A4C12		
A4C51	Cap, 10 µF, same as A4C11		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A4C52	Cap, 0.1 μF, same as A4C12		
A4C53	Cap, 10 μF, same as A4C11		
A4C54	Cap, 0.1 μF, same as A4C12		
A4C55	Cap, 0.1 μF, same as A4C12		
A4C56	Cap, 0.1 μF, same as A4C12		
A4C57	Cap, 10 μF, same as A4C11		
A4C58	Cap, 500 pF ±5%, 100 wvdc, silver mica	610 20500 21	1
A4C59	Cap, 0.1 μF, same as A4C12		
A4C60	Cap, 0.1 μF, same as A4C12		
A4C61	Cap, 0.1 μF, same as A4C12		
A4C62	Cap, 10 μF, same as A4C11		
A4C63	Cap, 0.1 μF, same as A4C12		
A4C64	Cap, 22 μF, ±20%, 6 wvdc, tantalum	640 00001 02	2
A4C65	Cap, 22 μF, same as A4C64		
A4C66	Cap, 0.1 μF, same as A4C12		
A4C67	Cap, 0.1 μF, same as A4C12		
A4C68	Cap, 0.01 μF, ±10%, 50 wvdc, mono	600 00015 02	1
A4C69	Cap, 0.1 μF, same as A4C12		
A4CR1	Diode, Quad Schottky Barrier	410 00043 00	2
A4CR2	Diode, same as A4CR1		
A4CR3	Diode, type 1N914A	410 00015 00	1
A4FL1	Filter, Crystal, 3100 Hz B.W. at 5 MHz (used in units with 3100 Hz selectivity)	760 00023 00	1
A4FL1	Filter, Crystal, C-Message B.W. at 5 MHz (used in units with C-Message selectivity)	760 00024 00	1
A4FL2	Filter, Crystal, 50 Hz B.W. at 455 kHz (used in units with 50 Hz selectivity)	760 00027 00	1
A4FL2	Filter, Crystal, 100 Hz B.W. at 455 kHz (used in units with 100 Hz selectivity)	760 00011 01	1
A4FL3	Filter, L.C., 10 kHz B.W. at 455 kHz	761 00009 00	1
A4I1	Integrated Circuit, type LF356N	431 00077 01	1
A4I2	Integrated Circuit, TO-92 LM340LAZ-10	431 00060 00	2
A4I3	NOT USED		
A4I4	IC, TO-92 LM340LAZ-10, same as A4I2		
A4I5	Integrated Circuit, type 4067B	430 00104 10	1
A4I6	Integrated Circuit, J-FET LF357N	431 00069 01	2
A4I7	Integrated Circuit, type 4066	430 00094 00	2
A4I8	Integrated Circuit, 4066, same as A4I7		
A4I9	Integrated Circuit, LF357N, same as A4I6		
A4I10	Integrated Circuit, type MC1350P	431 00025 01	1
A4I11	NOT USED		
A4J1	Jack, Phono, Printed Circuit	812 00059 00	4
A4J2	Jack, same as A4J1		
A4J3	Jack, same as A4J1		
A4J4	Jack, same as A4J1		
A4L1	Coil Assembly, 6.9 μH	701 00051 02	1
A4L2	Coil Assembly, 5.6 μH	701 00053 02	2
A4L3	Coil Assembly, 5.0 μH	701 00054 02	1
A4L4	Coil Assembly, 5.6 μH, same as A4L2		
A4L5	Coil Assembly, 9.9 μH	701 00055 02	1
A4L6	Parasitic Suppressor	701 00056 00	1
A4Q1	Transistor, Quad PNP, type MPQ3799	400 00047 00	1
A4Q2	Transistor, NPN, type MPSA18	400 00037 00	2
A4Q3	Transistor, FET, type 40841, selected	400 00040 01	1
A4Q4	Transistor, NPN, type MPSA18, MOT.	400 00037 01	2
A4Q5	Transistor, MPSA18, same as A4Q2		
A4Q6	Transistor, MPSA18, same as A4Q4		
A4Q7	Transistor, NPN, type 2N4124	400 00018 00	1
A4Q8	Transistor, PNP, type 2N5087, FAIRCHILD	400 00021 02	1

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A4R1	Res, 383 ohms ±1%, 1/8 W, metal film	511 23830 00	1
A4R2	Res, 121 ohms ±1%, 1/8 W, metal film	511 21210 00	1
A4R3	Res, 5100 ohms ±5%, 1/4 W, carbon film	500 00512 00	2
A4R4	Res, 4700 ohms ±5%, 1/4 W, carbon film	500 00472 00	6
A4R5	Res, 6200 ohms ±5%, 1/4 W, carbon film	500 00622 00	1
A4R6	Res, 3300 ohms ±5%, 1/4 W, carbon film	500 00332 00	2
A4R7	Res, 1300 ohms ±5%, 1/4 W, carbon film	500 00132 00	1
A4R8	Res, 390 ohms ±5%, 1/4 W, carbon film	500 00391 00	2
A4R9	Res, 390 ohms same as A4R8		
A4R10	Res, 5 k ohms ±20%, 3/4 W, cermet	542 00020 01	1
A4R11	Res, 22 ohms ±5%, 1/4 W, carbon film	500 00220 00	10
A4R12	Res, 100 ohms ±5%, 1/4 W, carbon film	500 00101 00	2
A4R13	Res, 100 ohms, same as A4R12		
A4R14	Res, 4990 ohms ±1%, 1/8 W, metal film	511 24991 00	4
A4R15	Res, var, 500 ohms ±10%, 1/2 W, cermet	542 00018 01	1
A4R16	Res, 4990 ohms, same as A4R14		
A4R17	Res, 510 ohms ±5%, 1/4 W, carbon film	500 00511 00	1
A4R18	Res, 470 k ohms, ±5%, 1/4 W, carbon film	500 00474 00	2
A4R19	Res, 5100 ohms, same as A4R3		
A4R20	Res, 470 k ohms, same as A4R18		
A4R21	Res, 4990 ohms, same as A4R14		
A4R22	Res, 4990 ohms, same as A4R14		
A4R23	Res, 10 k ohms ±5%, 1/4 W, carbon film	500 00103 00	2
A4R24	Res, 91 k ohms ±5%, 1/4 W, carbon film	500 00913 00	1
A4R25	Res, 100 k ohms ±5%, 1/4 W, carbon film	500 00104 00	1
A4R26	Res, 22 ohms, same as A4R11		
A4R27	NOT USED		
A4R28	Res, 150 ohms ±5%, 1/4 W, carbon film	500 00151 00	1
A4R29	Res, 22 ohms, same as A4R11		
A4R30	Res, 4700 ohms, same as A4R4		
A4R31	Res, 4700 ohms, same as A4R4		
A4R32	Res, 220 ohms ±5%, 1/4 W, carbon film	500 00221 00	2
A4R33	Res, 4700 ohms, same as A4R4		
A4R34	Res, 4700 ohms, same as A4R4		
A4R35	Res, 47 ohms ±5%, 1/4 W, carbon film	500 00470 00	1
A4R36	Res, 22 ohms, same as A4R11		
A4R37	Res, 220 ohms, same as A4R32		
A4R38	Res, 49.9 ohms ±0.1%, 1/2 W, metal film	513 04998 00	3
A4R39	Res, 226 ohms ±1%, 1/8 W, metal film	511 02260 00	1
A4R40	Res, 49.9 ohms, same as A4R38		
A4R41	Res, 226 ohms ±0.1%, 1/2 W, metal film	513 02260 00	1
A4R42	Res, 54.9 k ohms ±1%, 1/8 W, metal film	511 25492 00	1
A4R43	Res, 49.9 ohms, same as A4R38		
A4R44	Res, 221 ohms ±0.1%, 1/2 W, metal film	513 02210 00	1
A4R45	Res, 9760 ohms ±1%, 1/8 W, metal film	511 29761 00	1
A4R46	Res, 63.4 ohms ±0.1%, 1/2 W, metal film	513 06348 00	1
A4R47	Res, 113 ohms ±0.1% 1/2 W, metal film	513 01130 00	2
A4R48	Res, 28.7 k ohms ±1%, 1/8 W, metal film	511 22872 00	1
A4R49	Res, 64.9 ohms ±0.1%, 1/2 W, metal film	513 06498 00	1
A4R50	Res, 113 ohms, same as A4R47		
A4R51	Res, 7870 ohms ±1%, 1/8 W, metal film	511 27871 00	1
A4R52	Res, 66.5 ohms ±0.1%, 1/2 W, metal film	513 06658 00	1
A4R53	Res, 107 ohms ±0.1%, 1/2 W, metal film	513 01070 00	1
A4R54	Res, 8450 ohms ±1%, 1/8 W, metal film	511 28451 00	1
A4R55	Res, 68.1 ohms ±0.1%, 1/2 W, metal film	513 06818 00	1
A4R56	Res, 105 ohms ±0.1%, 1/2 W, metal film	513 01050 00	1
A4R57	Res, 24.3 k ohms ±1%, 1/8 W, metal film	511 22432 00	1
A4R58	Res, 69.8 ohms ±0.1%, 1/2 W, metal film	513 06988 00	1
A4R59	Res, 100 ohms ±0.1%, 1/2 W, metal film	513 01000 00	1
A4R60	Res, 4120 ohms ±1%, 1/8 W, metal film	511 24121 00	1
A4R61	Res, 71.5 ohms ±0.1%, 1/2 W, metal film	513 07158 00	1

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A4R62	Res, 97.6 ohms ±0.1%, 1/2 W, metal film	513 09768 00	1
A4R63	Res, 8870 ohms ±1%, 1/8 W, metal film	511 28871 00	1
A4R64	Res, 137 ohms ±0.1%, 1/2 W, metal film	513 01370 00	1
A4R65	Res, 8250 ohms ±1%, 1/8 W, metal film	511 28251 00	1
A4R66	Res, 59.0 ohms ±0.1%, 1/2 W, metal film	513 05908 00	1
A4R67	Res, 143 ohms ±0.1%, 1/2 W, metal film	513 01430 00	1
A4R68	Res, 294 k ohms ±1%, 1/8 W, metal film	511 22943 00	1
A4R69	Res, 57.6 ohms ±0.1%, 1/2 W, metal film	513 05768 00	1
A4R70	Res, 47 k ohms ±5%, 1/4 W, carbon film	500 00473 00	6
A4R71	Res, 47 k ohms, same as A4R70		
A4R72	Res, 47 k ohms, same as A4R70		
A4R73	Res, 47 k ohms, same as A4R70		
A4R74	Res, 22 ohms, same as A4R11		
A4R75	Res, 47 k ohms, same as A4R70		
A4R76	Res, 1 Meg ohm ±5%, 1/4 W, carbon film	500 00105 00	4
A4R77	Res, 1 Meg ohm, same as A4R76		
A4R78	Res, 22 ohms, same as A4R11		
A4R79	Res, 300 ohms ±5%, 1/4 W, carbon film	500 00301 00	2
A4R80	Res, 1800 ohms ±5%, 1/4 W, carbon film	500 00182 00	2
A4R81	Res, 464 ohms ±1%, 1/8 W, metal film	511 24640 00	1
A4R82	Res, 732 ohms ±1%, 1/8 W, metal film	511 27320 00	1
A4R83	Res, var, 200 ohms ±10%, 1/2 W, cermet	542 00018 00	1
A4R84	Res, 270 ohms ±5%, 1/4 W, carbon film	500 00271 00	1
A4R85	Res, 560 ohms ±5%, 1/4 W, carbon film	500 00561 00	1
A4R86	Res, 180 ohms ±5%, 1/4 W, carbon film	500 00181 00	1
A4R87	Res, 47 k ohms, same as A4R70		
A4R88	Res, 1 Meg ohm, same as A4R76		
A4R89	Res, 1 Meg ohm, same as A4R76		
A4R90	Res, 22 ohms, same as A4R11		
A4R91	Res, 300 ohms, same as A4R79		
A4R92	Res, 1800 ohms, same as A4R80		
A4R93	Res, 22 ohms, same as A4R11		
A4R94	Res, 22 ohms, same as A4R11		
A4R95	NOT USED		
A4R96	Res, 20 k ohms ±5%, 1/4 W, carbon film	500 00203 00	1
A4R97	Res, 10 k ohms, same as A4R23		
A4R98	Res, 15 k ohms ±5%, 1/4 W, carbon film	500 00153 00	1
A4R99	Res, 18 k ohms ±5%, 1/4 W, carbon film	500 00183 00	1
A4R100	Res, 1000 ohms ±5%, 1/4 W, carbon film	500 00102 00	1
A4R101	Res, 22 ohms, same as A4R11		
A4R102	Res, 51 ohms ±5%, 1/4 W, carbon film	500 00510 00	1
A4R103	Res, 68 k ohms ±5%, 1/4 W, carbon film	500 00683 00	1
A4R104	Res, 3900 ohms ±5%, 1/4 W, carbon film	500 00392 00	2
A4R105	Res, 4700 ohms, same as A4R4		
A4R106	Res, 3900 ohms, same as A4R104		
A4R107	Res, 3300 ohms, same as A4R6		
A4R108	Res, var, 100 k ohms ±10%, 1/2 W, cermet	542 00018 06	1
A4T1	Transformer, RF, 5 MHz	700 00047 02	1
A4T2	Transformer, 1st mixer input	700 00052 00	2
A4T3	Transformer, same as A4T2		
A4T4	Transformer, RF, 5 MHz	700 00049 02	1
A4T5	Transformer, IF, 455 kHz	700 00048 02	2
A4T6	Transformer, same as A4T5		
	MONITOR ASSEMBLY A5		
A5	Circuit Card Assembly, Monitor	110 00079 03	1
A5C1	Cap, 0.1 μF (+80, −20%) 25 wvdc, ceramic	600 00003 12	2
A5C2	Cap, 10 μF, ±20%, 15 wvdc, tantalum	640 00001 01	1
A5C3	Cap, 100 pF ±5%, 100 wvdc, mica	610 20100 21	1
A5C4	Cap, 0.1 μF, same as A5C1		
A5C5	Cap, 22 pF ±1%, 100 wvdc, mica	610 20022 01	1

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A5C6	Cap, 0.01 μF (+80, −20%) 25 wvdc, ceramic	600 00003 00	4
A5C7	Cap, 0.01 μF, same as A5C6		
A5C8	Cap, 0.01 μF, same as A5C6		
A5C9	Cap, 0.01 μF, same as A5C6		
A5C10	Cap, 1 μF ±20%, 35 wvdc, tantalum	640 00001 03	1
A5C11	Cap, 22 μF (+50, −10%) 16 wvdc Al. elct'c	630 00001 01	1
A5C12	Cap, 22 μF, 35 wvdc, alum elect'c	630 00004 00	1
A5CR1	Diode, germanium, 1N277	410 00005 00	2
A5CR2	Diode, 1N277, same as A5CR1		
A5I1	NOT USED		
A5I2	Integrated Circuit, type LM377N	431 00058 01	1
A5L1	Coil, rf, 500 μH	701 00017 01	1
A5Q1	Transistor, FET, 2N5484 selected	400 00001 01	1
A5Q2	Transistor, PNP, silicon, 2N3702	400 00012 00	1
A5R1	NOT USED		
A5R2	NOT USED		
A5R3	Res, 1 Meg ohm ±5%, 1/4 W, carbon	500 00105 00	3
A5R4	Res, 1000 ohms ±5%, 1/4 W, carbon	500 00102 00	3
A5R5	Res, 2200 ohms ±5%, 1/4 W, carbon	500 00222 00	1
A5R6	Res, 2400 ohms ±5%, 1/4 W, carbon	500 00242 00	1
A5R7	Res, 1000 ohms, same as A5R4		
A5R8	Res, 1000 ohms, same as A5R4		
A5R9	Res, 4700 ohms ±5%, 1/4 W, carbon	500 00472 00	2
A5R10	Res, 4700 ohms, same as A5R9		
A5R11	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	1
A5R12	Res, 3900 ohms ±5%, 1/4 W, carbon	500 00392 00	1
A5R13	Res, 1 Meg ohms, same as A5R3		
A5R14	Res, 5600 ohms ±5%, 1/4 W, carbon	500 00562 00	1
A5R15	Res, 100 k ohms ±5%, 1/4 W, carbon	500 00104 00	1
A5R16	Res, 1 Meg ohm, same as A5R3		
A5R17	Res, 47 ohms ±5%, 1/4 W, carbon	500 00470 00	1
A5S1	Switch, rotary, wafer only	720 00021 01	1
A5S1	Switch, rotary, detent only	720 00062 00	1
A5Y1	Crystal, 456.500 kHz	765 00014 00	1
A5Y2	Crystal, 453.500 kHz	765 00013 00	1
	FREQUENCY HOUSING COVER ASSEMBLY A6		
A6	Frequency Housing Cover Assembly	120 00189 00	1
	The Frequency Housing Cover Assembly consists of Circuit Card Assemblies A8 and A11.		
	FREQUENCY DISPLAY ASSEMBLY A7		
A7	Circuit Card Assembly, Frequency Display	110 00139 00	1
A7C1	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	2
A7C2	Cap, 0.1 μF, same as A7C1		
A7DH1	Heater, LCD	440 00003 01	1
A7I1	Integrated Circuit, type MC14553CP	430 00002 15	2
A7I2	Integrated Circuit, MC14553CP, same as A7I1		
A7I3	Integrated Circuit, type 4543B	430 00072 10	6
A7I4	Integrated Circuit, 4543B, same as A7I3		
A7I5	Integrated Circuit, 4543B, same as A7I3		
A7I6	Integrated Circuit, 4543B, same as A7I3		
A7I7	Integrated Circuit, 4543B, same as A7I3		
A7I8	Integrated Circuit, 4543B, same as A7I3		
A7I9	Integrated Circuit, type 4001B	430 00058 12	1
A7I10	Integrated Circuit, type 4030B	430 00052 10	1
A7I11	Integrated Circuit, 6-digit LCD	430 00098 00	1
A7J1	Receptacle, 8-pin	813 00021 08	2

PARTS LIST

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A7J2	Receptacle, 8-pin, same as A7J1		
A7R1	Res, 100 k ohms ±5%, 1/4 W, carbon	500 00104 00	1
	TIMING/COUNTER INPUT ASSEMBLY A8		
A8	Circuit Card Assembly, Timing/Counter Input Serial Nos. 101-200 only	110 00140 00	1
A8	Circuit Card Assembly, Timing/Counter Input Serial Nos. 201 up	110 00140 01	1
A8C1	Cap, 0.01 μF ±10%, 50 wvdc, mono	600 00015 02	3
A8C2	Cap, 0.01 μF, same as A8C1		
A8C3	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	11
A8C4	Cap, 0.01 μF, same as A8C1		
A8C5	Cap, 0.1 μF, same as A8C3		
A8C6	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	3
A8C7	Cap, 0.1 μF, same as A8C3		
A8C8	Cap, 10 μF, same as A8C6		
A8C9	Cap, 0.1 μF, same as A8C3		
A8C10	Cap, 10 μF, same as A8C6		
A8C11	Cap, 0.1 μF, same as A8C3		
A8C12	Cap, 0.1 μF, same as A8C3		
A8C13	Cap, 0.1 μF, same as A8C3		
A8C14	Cap, 0.1 μF, same as A8C3		
A8C15	Cap, 0.1 μF, same as A8C3		
A8C16	Cap, 22 pF ±5%, 100 wvdc, silver mica	610 20022 21	1
A8C17	Cap, 0.1 μF, same as A8C3		
A8C18	Cap, 0.1 μF, same as A8C3		
A8I1	Integrated Circuit, type 4017B	430 00050 10	4
A8I2	Integrated Circuit, 4017B, same as A8I1		
A8I3	Integrated Circuit, type 4518B	430 00009 10	3
A8I4	Integrated Circuit, type 4085B	430 00102 10	2
A8I5	Integrated Circuit, 4518B, same as A8I3		
A8I6	Integrated Circuit, type 4023B	430 00056 12	1
A8I7	Integrated Circuit, type 4013B	430 00048 10	6
A8I8	Integrated Circuit, type 4001B	430 00058 12	2
A8I9	Integrated Circuit, type 74C73 Serial Nos. 101-200 only	430 00064 00	1
A8I9	Integrated Circuit, type 74C107 Serial Nos. 201 up	430 00112 00	1
A8I10	Integrated Circuit, type 4011B	430 00046 12	1
A8I11	Integrated Circuit, 4013B, same as A817		
A8I12	Integrated Circuit, 4518B, same as A813		
A8I13	Integrated Circuit, 4017B, same as A811		
A8I14	Integrated Circuit, type 4020B	430 00060 10	1
A8I15	Integrated Circuit, 4013B, same as A817		
A8I16	Integrated Circuit, 4013B, same as A817		
A8I17	Integrated Circuit, 4013B, same as A817		
A8I18	Integrated Circuit, type 4520B	430 00101 10	1
A8I19	Integrated Circuit, type LM393N	431 00066 01	1
A8I20	Integrated Circuit, type 74LS86	430 00075 00	1
A8I21	Integrated Circuit, 4001B, same as A8I8		
A8I22	Integrated Circuit, type 74LS74	430 00077 00	1
A8I23	Integrated Circuit, type 74LS175	430 00076 00	1
A8I24	Integrated Circuit, 4017B, same as A8I1		
A8I25	Integrated Circuit, 4085B, same as A8I4		
A8I26	Integrated Circuit, 4013B, same as A8I7		
A8I27	Integrated Circuit, type 4030B	430 00052 10	1
A8I28	Integrated Circuit, type 74C175	430 00068 00	1
A8I29	Integrated Circuit, type 78LO5	431 00009 00	1
A8J1	8-pin receptacle	813 00021 08	1
A8P1	8-pin right angle header assy	812 00082 08	2

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A8P2	8-pin header assy, same as A8P1		
A8Q1	Transistor, silicon, NPN, type 2N3704	400 00013 00	1
A8R1	Res, 20 k ohms ±5%, 1/4 W, carbon	500 00203 00	1
A8R2	Res, 30 k ohms ±5%, 1/4 W, carbon	500 00303 00	4
A8R3	Res, 820 ohms ±5%, 1/4 W, carbon	500 00821 00	1
A8R4	NOT USED		
A8R5	Res, 100 k ohms ±5%, 1/4 W, carbon	500 00104 00	2
A8R6	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	1
A8R7	NOT USED		
A8R8	NOT USED		
A8R9	Res, 4700 ohms ±5%, 1/4 W, carbon	500 00472 00	1
A8R10	Res, 1000 ohms ±5%, 1/4 W, carbon	500 00102 00	1
A8R11	Res, 30 k ohms, same as A8R2		
A8R12	Res, 100 k ohms, same as A8R5		
A8R13	Res, 30 k ohms, same as A8R2		
A8R14	Res, 1 Meg ohm ±5%, 1/4 W, carbon	500 00105 00	1
A8R15	Res, 30 k ohms, same as A8R2		
A8R16	Res, 1100 ohms ±5%, 1/4 W, carbon	500 00112 00	1
	1st L.O. ASSEMBLY A9		
A9	Circuit Card Assembly, 1st L.O.	110 00112 01	1
A9C1	NOT USED		
A9C2	Cap, 18 pF ±5%, 100 wvdc, silver mica	610 20018 21	1
A9C3	Cap, 22 pF ±5%, N330	601 00004 03	2
A9C4	Cap, 500 pF ±5%, 100 wvdc, silver mica	610 20500 21	1
A9C5	Cap, 10 pF ±5%, 100 wvdc, silver mica	610 20010 21	1
A9C6	Cap, 30 pF ±1%, 100 wvdc, silver mica	610 20030 01	1
A9C7	Cap, 250 pF ±5%, 100 wvdc, silver mica	610 20250 21	1
A9C8	Cap, 22 pF, N330, same as A9C3		
A9C9	Cap, 75 pF ±1%, 100 wvdc, silver mica	610 20075 01	1
A9C10	Cap, 30 pF ±5%, N470	601 00002 46	1
A9C11	Cap, 150 pF ±1%, 100 wvdc, silver mica	610 20150 01	1
A9C12	Cap, 27 pF ±5%, N330	601 00002 48	1
A9C13	Cap, 27 pF ±5%, N470	601 00002 49	1
A9C14	Cap, 600 pF ±5%, 100 wvdc, silver mica	610 20600 21	2
A9C15	Cap, 600 pF, same as A9C14		
A9C16	Cap, 56 pF ±5%, N750	601 00002 39	2
A9C17	Cap, 56 pF, same as A9C16		
A9C18	Cap, 75 pF ±5%, 100 wvdc, silver mica	610 20075 21	1
A9C19	Cap, 120 pF ±5%, 100 wvdc, silver mica	610 20120 21	1
A9C20	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	1
A9C21	Cap, 0.01 μF ±20%, 100 wvdc, ceramic	600 00001 03	4
A9C22	Cap, 0.01 μF, same as A9C21		
A9C23	Cap, 0.01 μF, same as A9C21		
A9C24	Cap, 0.01 μF, same as A9C21		
A9C25	Cap, 10 pF ±5%, N080	601 00002 01	1
A9CR1	Diode, type 1N914	410 00014 00	1
A9CR2	Diode, type MV1404	410 00045 00	1
A9I1	IC, Voltage Regulator	431 00073 00	1
A9L1	Coil, var., 2.3 μH, Nom.	701 00040 00	1
A9L2	Coil, RF, 80 μH	701 00015 02	1
A9Q1	Transistor, NPN, type 2N918	400 00044 00	2
A9Q2	Transistor, 2N918, same as A9Q1		
A9R1	Res, 100 k ohms ±5%, 1/4 W, carbon	500 00104 00	1
A9R2	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	4
A9R3	Res, 10 k ohms, same as A9R2		
A9R4	Res, 39 ohms ±5%, 1/4 W, carbon	500 00390 00	1
A9R5	Res, 2400 ohms ±5%, 1/4 W, carbon	500 00242 00	4
A9R6	Res, 2400 ohms, same as A9R5		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A9R7	Res, 2400 ohms, same as A9R5		
A9R8	Res, 2400 ohms, same as A9R5		
A9R9	Res, 1600 ohms ±5%, 1/4 W, carbon	500 00162 00	1
A9R10	Res, 10 k ohms, same as A9R2		
A9R11	Res, 10 k ohms, same as A9R2		
A9R12	Res, 30 k ohms ±5%, 1/4 W, carbon	500 00303 00	1
A9R13	Res, var. 50 k ohms ±10%, 1/2 W, cermet	542 00003 07	1
A9S1	Switch, rotary, detent/wafer	720 00067 00	1
	1st L.O. BUFFER/AMP ASSEMBLY A10		
A10	Circuit Card Assembly, 1st L.O. Buffer/Amp	110 00141 00	1
A10C1	Cap, 15 pf ±5%, 100 wvdc, mica	610 20015 21	1
A10C2	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	13
A10C3	Cap, 0.1 μF, same as A10C2		
A10C4	Cap, 0.1 μF, same as A10C2		
A10C5	Cap, 0.1 μF, same as A10C2		
A10C6	Cap, 0.1 μF, same as A10C2		
A10C7	Cap, 0.1 μF, same as A10C2		
A10C8	Cap, 0.1 μF, same as A10C2		
A10C9	Cap, 0.1 μF, same as A10C2		
A10C10	Cap, 0.1 μF, same as A10C2		
A10C11	Cap, 0.1 μF, same as A10C2		
A10C12	Cap, 0.1 μF, same as A10C2		
A10C13	Cap, 0.1 μF, same as A10C2		
A10C14	Cap, 0.1 μF, same as A10C2		
A10C15	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	1
A10CR1	Diode, type 1N914A	410 00015 00	5
A10CR2	Diode, 1N914A, same as A10CR1		
A10CR3	Diode, 1N914A, same as A10CR1		
A10CR4	Diode, 1N914A, same as A10CR1		
A10CR5	Diode, 1N914A, same as A10CR1		
A10I1	Integrated Circuit, type 78LO5	431 00009 00	1
A10Q1	Transistor, NPN, type 2N4124	400 00018 00	4
A10Q2	Transistor, 2N4124, same as A10Q1		
A10Q3	Transistor, NPN, type MPS2369	400 00048 00	2
A10Q4	Transistor, MPS2369, same as A10Q3		
A10Q5	Transistor, 2N4124, same as A10Q1		
A10Q6	Transistor, PNP, type 2N4126	400 00042 00	1
A10Q7	Transistor, 2N4124, same as A10Q1		
A10R1	Res, 2000 ohms ±5%, 1/4 W, carbon film	500 00202 00	4
A10R2	Res, 2000 ohms, same as A10R1		
A10R3	Res, 360 ohms ±5%, 1/4 W, carbon film	500 00361 00	2
A10R4	Res, 62 ohms ±5%, 1/4 W, carbon film	500 00620 00	2
A10R5	Res, 180 ohms ±5%, 1/4 W, carbon film	500 00181 00	2
A10R6	Res, 1000 ohms ±5%, 1/4 W, carbon film	500 00102 00	1
A10R7	Res, 2000 ohms, same as A10R1		
A10R8	Res, 3300 ohms ±5%, 1/4 W, carbon film	500 00332 00	1
A10R9	Res, 180 ohms, same as A10R5		
A10R10	Res, 62 ohms, same as A10R4		
A10R11	Res, 51 ohms ±5%, 1/4 W, carbon film	500 00510 00	1
A10R12	Res, 360 ohms, same as A10R3		
A10R13	Res, 300 ohms ±5%, 1/4 W, carbon film	500 00301 00	1
A10R14	Res, 1300 ohms ±5%, 1/4 W, carbon film	500 00132 00	1
A10R15	Res, 2400 ohms ±5%, 1/4 W, carbon film	500 00242 00	1
A10R16	Res, 270 ohms ±5%, 1/4 W, carbon film	500 00271 00	1
A10R17	Res, 100 ohms ±5%, 1/4 W, carbon film	500 00101 00	1
A10R18	Res, 22 ohms ±5%, 1/4 W, carbon film	500 00220 00	1
A10R19	NOT USED		
A10R20	Res, 470 ohms ±5%, 1/4 W, carbon film	500 00471 00	1
A10R21	Res, 2000 ohms, same as A10R1		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A10R22	Res, 4300 ohms ±5%, 1/4 W, carbon film	500 00432 00	1
	PHASE LOCK LOOPS ASSEMBLY A11		
A11	Circuit Card Assembly, Phase Lock Loops Serial Nos. 101-200 only	110 00142 00	1
A11	Circuit Card Assembly, Phase Lock Loops Serial Nos. 201 up	110 00142 01	1
A11C1	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	3
A11C2	Cap, 0.22 μF ±10%, 50 wvdc, mono	600 00015 00	2
A11C3	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	5
A11C4	Cap, 22 μF ±20%, 16 wvdc, tantalum	640 00001 05	1
A11C5	Cap, 0.22 μF, same as A11C2		
A11C6	Cap, 0.1 μF, same as A11C3		
A11C7	Cap, 0.1 μF, same as A11C3		
A11C8	Cap, 10 μF, same as A11C1		
A11C9	Cap, 0.1 μF, same as A11C3		
A11C10	Cap, 0.1 μF, same as A11C3		
A11C11	Cap, 10 μF, same as A11C1		
A11I1	Integrated Circuit, type 4518B	430 00009 10	3
A11I2	Integrated Circuit, type 4023B	430 00056 12	1
A11I3	Integrated Circuit, type 4013B	430 00048 10	2
A11I4	Integrated Circuit, 4518B, same as A11I1		
A11I5	Integrated Circuit, type 4520B	430 00101 10	1
A11I6	Integrated Circuit, 4013B, same as A11I3		
A11I7	Integrated Circuit, type 74C73 Serial Nos. 101-200 only	430 00064 00	1
A11I7	Integrated Circuit, type 74C107 Serial Nos. 201 up	430 00112 00	1
A11I8	Integrated Circuit, type 4015B	430 00049 10	1
A11I9	Integrated Circuit, 4518B, same as A11I1		
A11I10	Integrated Circuit, type 4030B	430 00052 10	1
A11P1	8-pin right angle header assy	812 00082 08	1
A11R1	Res, 4.7 Meg ohms ±5%, 1/4 W, carbon	500 00475 00	1
A11R2	Res, 392 k ohms ±1%, 1/8 W, metal film	511 23923 00	2
A11R3	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	1
A11R4	Res, 270 k ohms ±5%, 1/4 W, carbon	500 00274 00	1
A11R5	Res, 200 k ohms ±5%, 1/4 W, carbon	500 00204 00	2
A11R6	Res, 200 k ohms, same as A11R5		
A11R7	Res, 392 k ohms, same as A11R2		
A11R8	Res, 20 k ohms ±5%, 1/4 W, carbon	500 00203 00	1
A11YM1	Oscillator, Crystal	490 00001 00	1
	2nd L.O. ASSEMBLY A12		
A12	Circuit Card Assembly, 2nd L.O.	110 00143 00	1
A12C1	Cap, 68 pF ±5%, 100 wvdc, silver mica	610 20068 21	1
A12C2	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	1
A12C3	Cap, 500 pF ±5%, 100 wvdc, silver mica	610 20500 21	1
A12C4	Cap, 200 pF ±5%, 100 wvdc, silver mica	610 20200 21	1
A12C5	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	4
A12C6	Cap, 0.01 μF ±10%, 50 wvdc, mono	600 00015 02	1
A12C7	Cap, 47 pF ±5%, 100 wvdc, silver mica	610 20047 21	1
A12C8	Cap, 0.1 μF, same as A12C5		
A12C9	Cap, 0.1 μF, same as A12C5		
A12C10	Cap, 0.1 μF, same as A12C5		
A12CR1	Diode, volt var. cap, type MV1405	410 00032 01	1
A12I1	Integrated Circuit, type 78LO8	431 00073 00	1
A12I2	Integrated Circuit, type 4001B	430 00058 12	1
A12L1	Coil, RF, 27 μH	701 00033 01	1

PARTS LIST

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A12Q1	Transistor, NPN, type 2N3710, selected	400 00002 01	1
A12Q2	Transistor, NPN, type 2N3704	400 00013 00	1
A12Q3	Transistor, PNP, type 2N3702	400 00012 00	1
A12R1	Res, 100 k ohms ±5%, 1/4 W, carbon	500 00104 00	2
A12R2	Res, 33 k ohms ±5%, 1/4 W, carbon	500 00333 00	1
A12R3	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	1
A12R4	Res, 1000 ohms ±5%, 1/4 W, carbon	500 00102 00	1
A12R5	Res, 4700 ohms ±5%, 1/4 W, carbon	500 00472 00	1
A12R6	Res, 100 k ohms, same as A12R1		
A12R7	Res, 100 ohms ±5%, 1/4 W, carbon	500 00101 00	1
A12R8	Res, 33 ohms ±5%, 1/4 W, carbon	500 00330 00	1
A12Y1	Crystal, Quartz, 4545 kHz, ±0.005%	765 00007 00	1
	CALIBRATION OSC ASSEMBLY A14		
A14	Circuit Card Assembly, Calibration Osc	110 00149 00	1
A14C1	Cap, 18 pF ±5%, 100 wvdc, silver mica	610 20018 21	1
A14C2	Cap, 650 pF ±5%, 100 wvdc, silver mica	611 20650 21	1
A14C3	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	2
A14C4	Cap, 10 μF, ±20%, 15 wvdc, tantalum	640 00001 01	1
A14C5	Cap, 0.1 μF, same as A14C3		
A14I1	Integrated Circuit, type 4001B	430 00058 12	1
A14I2	Integrated Circuit, TO-92 LM329BZ	431 00084 00	1
A14R1	Res, 2000 ohms ±1%, 1/8 W, metal film	511 22001 00	1
A14R2	Res, 1 Meg ohm ±5%, 1/4 W, carbon film	500 00105 00	1
A14R3	Res, 7500 ohms ±5%, 1/4 W, carbon film	500 00752 00	1
A14R4	Res, 57.6 k ohms ±1%, 1/8 W, metal film	511 25762 20	1
A14R5	Res, var, 20 k ohms ±20%, 1/2 W, cermet	542 00003 09	1
A14R6	Res, 187 ohms ±1%, 1/8 W, metal film	511 21870 20	1
A14Y1	Crystal, Quartz, 250 kHz ±0.01%	765 00011 00	1
	POWER SUPPLY ASSEMBLY A15		
A15	Power Supply Assembly A15 (115 vac operation)	120 00061 04	1
A15	Power Supply Assembly A15 (230 vac operation)	120 00061 05	1
	The Power Supply Assembly A15 consists of Circuit Card Assembly A1 and the following:		
A15CR1	Rectifier, Bridge, 200 PIV, 2 Amp	410 00025 00	1
A15F1	Fuse, MDL, Slo-blow, 3/8 A	723 00006 00	1
A15T1	Transformer, Power with P3 (used in units with 115 vac operation)	120 00063 00	1
A15T1	Transformer, Power with P3 (used in units with 230 vac operation)	120 00063 01	1
	1ST L.O. ASSEMBLY A16		
A16	1st L.O. Assembly	120 00187 00	1
	The 1st L.O. Assembly consists of circuit card assemblies A9, A10 and the following:		
A16C1	Cap, Air, var. 10-140 pF	650 00005 00	1
A16C2	Cap, Feed-thru, 0.001 μF	680 00003 00	2
A16C3	Cap, Feed-thru, 0.001 μF, same as A16C2		
A16C4	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	1
A16L1	Parasitic Suppressor	701 00066 00	1
	INPUT ASSEMBLY A17		
A17	Input Assembly	120 00204 00	1
A17	Input Assembly, C-MSG	120 00204 01	1
	The Input Assembly consists of Circuit Card Assemblies A2, A14 and A24		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
	ATTENUATOR ASSEMBLY A18		
A18	Attenuator Assembly The Attenuator Assembly consists of Circuit Card A3.	120 00191 00	1
	AUTO RANGING ASSEMBLY A19		
A19	Circuit Card Assembly, Auto Ranging	110 00144 00	1
A19C1	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	8
A19C2	Cap, 0.1 μF, same as A19C1		
A19C3	Cap, 0.1 μF, same as A19C1		
A19C4	Cap, 0.1 μF, same as A19C1		
A19C5	Cap, 0.1 μF, same as A19C1		
A19C6	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	3
A19C7	Cap, 0.1 μF, same as A19C1		
A19C8	Cap, 10 μF, same as A19C6		
A19C9	Cap, 0.1 μF, same as A19C1		
A19C10	Cap, 1 μF ±20%, 100 wvdc, mylar	620 00023 00	1
A19C11	Cap, 10 μF, same as A19C6		
A19C12	Cap, 0.1 μF, same as A19C1		
A19CR1	Diode, silicon, type 1N914A	410 00015 00	9
A19CR2	Diode, 1N914A, same as A19CR1		
A19CR3	Diode, 1N914A, same as A19CR1		
A19CR4	Diode, 1N914A, same as A19CR1		
A19CR5	Diode, 1N914A, same as A19CR1		
A19CR6	Diode, 1N914A, same as A19CR1		
A19CR7	Diode, 1N914A, same as A19CR1		
A19CR8	Diode, 1N914A, same as A19CR1		
A19CR9	Diode, 1N914A, same as A19CR1		
A19I1	Integrated Circuit, type 4029B	430 00063 10	1
A19I2	Integrated Circuit, type 4049UB	430 00107 11	1
A19I3	Integrated Circuit, type 4082B	430 00110 10	1
A19I4	Integrated Circuit, type 4071B	430 00108 10	1
A19I5	Integrated Circuit, type 4081B	430 00109 10	2
A19I6	Integrated Circuit, 4081B, same as A19I5		
A19I7	Integrated Circuit, type 4025B	430 00051 12	1
A19I8	Integrated Circuit, type 4030B	430 00052 10	1
A19I9	Integrated Circuit, type 4008B	430 00106 10	1
A19I10	Integrated Circuit, type 4585B	430 00111 10	1
A19I11	Integrated Circuit, type 4042B	430 00089 10	1
A19I12	Integrated Circuit, type LM324N	431 00016 01	1
A19I13	Integrated Circuit, TO-92, LM340LAZ-10	431 00060 00	1
A19J1	SKT, IC, 8-pin 0.110 lg	813 00006 00	1
A19J2	SKT, IC, 14-pin 0.110 lg	813 00006 02	1
A19P1	Plug, right angle, 8-pin	812 00082 08	1
A19Q1	Transistor, NPN, type 2N3704	400 00013 00	3
A19Q2	Transistor, 2N3704, same as A19Q1		
A19Q3	Transistor, PNP, type 2N5087	400 00021 00	1
A19Q4	Transistor, PNP, type 2N3702	400 00012 00	1
A19Q5	Transistor, 2N3704, same as A19Q1		
A19Q6	Transistor, NPN, type MPSA14, Darlington	400 00049 00	8
A19Q7	Transistor, MPSA14, same as A19Q6		
A19Q8	Transistor, MPSA14, same as A19Q6		
A19Q9	Transistor, MPSA14, same as A19Q6		
A19Q10	Transistor, MPSA14, same as A19Q6		
A19Q11	Transistor, MPSA14, same as A19Q6		
A19Q12	Transistor, MPSA14, same as A19Q6		
A19Q13	Transistor, MPSA14, same as A19Q6		
A19R1	Res, 100 k ohms ±5%, 1/4 W, carbon film	500 00104 00	13

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A19R2	Res, 100 k ohms, same as A19R1		
A19R3	Res, 100 k ohms, same as A19R1		
A19R4	Res, 100 k ohms, same as A19R1		
A19R5	Res, 100 k ohms, same as A19R1		
A19R6	Res, 47 k ohms ±5%, 1/4 W, carbon film	500 00473 00	4
A19R7	Res, 47 k ohms, same as A19R6		
A19R8	Res, 86.6 k ohms ±1%, 1/8 W, metal film	511 28662 00	1
A19R9	Res, 12.1 k ohms ±1%, 1/8 W, metal film	511 21212 00	1
A19R10	Res, 19.6 k ohms ±1%, 1/8 W, metal film	511 21962 00	1
A19R11	Res, 1330 ohms ±1%, 1/8 W, metal film	511 21331 00	1
A19R12	Res, 47.5 k ohms ±1%, 1/8 W, metal film	511 24752 00	1
A19R13	Res, 10 k ohms ±5%, 1/4 W, carbon film	500 00103 00	1
A19R14	Res, 52.3 k ohms ±1%, 1/8 W, metal film	511 25232 00	1
A19R15	Res, 1300 ohms ±5%, 1/4 W, carbon film	500 00132 00	1
A19R16	Res, 47 k ohms, same as A19R6		
A19R17	Res, 47 k ohms, same as A19R6		
A19R18	Res, 100 k ohms, same as A19R1		
A19R19	Res, 100 k ohms, same as A19R1		
A19R20	Res, 100 k ohms, same as A19R1		
A19R21	Res, 100 k ohms, same as A19R1		
A19R22	Res, 100 k ohms, same as A19R1		
A19R23	Res, 100 k ohms, same as A19R1		
A19R24	Res, 100 k ohms, same as A19R1		
A19R25	Res, 100 k ohms, same as A19R1		
	LEVEL DETECTOR ASSEMBLY A21		
A21	Circuit Card Assembly, Level Detector Serial Nos. 101-200 only	110 00146 00	1
A21	Circuit Card Assembly, Level Detector Serial Nos. 201 up	110 00146 01	1
A21	Circuit Card Assembly, Level Detector, C-MSG	110 00146 02	1
A21C1	Cap, 0.001 μF ±10%, 50 wvdc, mono	600 00015 03	1
A21C2	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	12
A21C3	Cap, 1.0 μF ±5%, 50 wvdc, MPF	620 00032 00	1
A21C4	Cap, 390 pF ±5%, 100 wvdc, silver mica	610 20390 21	1
A21C5	Cap, 0.1 μF, same as A21C2		
A21C6	Cap, 1.0 μF ±20%, 35 wvdc, tantalum	640 00001 03	4
A21C7	Cap, 1.0 μF, same as A21C6		
A21C8	Cap, 0.47 μF ±20%, 35 wvdc, tantalum	640 00001 06	1
A21C9	Cap, 1.0 μF, same as A21C6		
A21C10	Cap, 1.0 μF, same as A21C6		
A21C11	Cap, 0.1 μF, same as A21C2		
A21C12	Cap, 0.1 μF, same as A21C2		
A21C13	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	6
A21C14	Cap, 0.1 μF, same as A21C2		
A21C15	Cap, 0.1 μF, same as A21C2		
A21C16	Cap, 0.1 μF, same as A21C2		
A21C17	Cap, 10 μF, same as A21C13		
A21C18	Cap, 0.1 μF, same as A21C2		
A21C19	Cap, 10 μF, same as A21C13		
A21C20	Cap, 0.1 μF, same as A21C2		
A21C21	Cap, 0.1 μF, same as A21C2		
A21C22	Cap, 10 μF, same as A21C13		
A21C23	Cap, 0.1 μF, same as A21C2		
A21C24	Cap, 10 μF, same as A21C13		
A21C25	Cap, 10 μF, same as A21C13		
A21C26	Cap, 0.1 μF, same as A21C2		
A21C27	Cap, 100 μF ±10%, 25 wvdc, elect'c	630 00009 00	1
A21CR1	Diode, silicon, type 1N457	410 00031 00	1
A21CR2	Diode, type 1N914A	410 00015 00	3
A21CR3	Diode, 1N914A, same as A21CR2		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A21CR4	Diode, Stabistor 1N5179 Installed as required Serial Nos. 201 up	410 00041 00	1
A21CR5	Diode, 1N914A, same as A21CR2 Serial Nos. 201 up		
A21I1	Integrated Circuit, type 311N	431 00055 01	2
A21I2	Integrated Circuit, type 358N	431 00054 00	2
A21I3	Integrated Circuit, 311N, same as A21I1		
A21I4	Integrated Circuit, type 4081B	430 00109 10	1
A21I5	Integrated Circuit, type 4017B Serial Nos. 101-200 only	430 00050 10	3
A21I6	Integrated Circuit, type 4020B	430 00060 10	2
A21I7	Integrated Circuit, 4017B, same as A21I5		
A21I8	Integrated Circuit, type 4013B	430 00048 10	3
A21I9	Integrated Circuit, type 4518B	430 00009 10	1
A21I10	Integrated Circuit, 4013B, same as A21I8		
A21I11	Integrated Circuit, 4013B, same as A21I8		
A21I12	Integrated Circuit, type 4520B	430 00101 10	1
A21I13	Integrated Circuit, 4020B, same as A21I6		
A21I14	Integrated Circuit, 358N, same as A21I2		
A21I15	Integrated Circuit, 4017B, same as A21I5		
A21I16	Integrated Circuit, type 78L05	431 00009 00	1
A21J1	SKT IC 14-pin 0.110 1g	831 00006 02	1
A21Q1	Transistor, FET, 2N5484, selected	400 00001 01	1
A21Q2	Transistor, PNP, type 2N3702	400 00012 00	1
A21Q3	Transistor, NPN, type 2N3704	400 00013 00	2
A21Q4	Transistor, 2N3704, same as A21Q3		
A21Q5	Transistor, NPN, type 2N5308	400 00025 00	1
A21Q6	Transistor, PNP, type 2N5087	400 00021 00	1
A21R1	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	4
A21R2	Res, 1000 ohms ±5%, 1/4 W, carbon	500 00102 00	3
A21R3	Res, var. 5 k ohms ±10%, 1/2 W, cermet	542 00003 03	1
A21R4	Res, 100 k ohms ±5%, 1/4 W, carbon Serial Nos. 101-200 only	500 00104 00	3
A21R4	Res, 33 k ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00333 00	1
A21R5	Res, 10 k ohms, same as A21R1		
A21R6	Res, 1000 ohms, same as A21R2		
A21R7	Res, 30 k ohms ±5%, 1/4 W, carbon	500 00303 00	1
A21R8	Res, var. 50 k ohms ±10%, 1/2 W, cermet Serial Nos. 101-200 only	542 00003 07	1
A21R8	Res, var. 500 k ohms ±10%, 1/2 W, cermet Serial Nos. 201 up	542 00003 12	1
A21R9	Res, 4.7 Meg ohms ±5%, 1/4 W, carbon	500 00475 00	2
A21R10	Res, 4.7 Meg ohms, same as A21R9		
A21R11	Res, var. 500 ohms ±10%, 1/2 W, cermet	542 00003 00	1
A21R12	Res, 2870 ohms ±1%, 1/8 W, metal film	511 22871 30	1
A21R13	Res, 48.7 k ohms ±1%, 1/8 W, metal film	511 24872 10	1
A21R14	Res, 1000 ohms ±1%, 1/8 W, metal film	511 21001 10	1
A21R15	Res, 2000 ohms ±5%, 1/4 W, carbon	500 00202 00	4
A21R16	Res, 100 k ohms ±1%, 1/8 W, metal film	511 21003 00	1
A21R17	Res, 22 k ohms ±5%, 1/4 W, carbon	500 00223 00	1
A21R18	Res, 11 k ohms ±5%, 1/4 W, carbon	500 00113 00	1
A21R19	Res, 28 k ohms ±1%, 1/8 W, metal film	511 22802 00	1
A21R20	Res, 4700 ohms ±5%, 1/4 W, carbon	500 00472 00	2
A21R21	Res, 47 k ohms ±5%, 1/4 W, carbon	500 00473 00	2
A21R22	Res, 43 k ohms ±5%, 1/4 W, carbon	500 00433 00	1
A21R23	Res, 91 k ohms ±5%, 1/4 W, carbon	500 00913 00	1
A21R24	Res, 2000 ohms, same as A21R15		
A21R25	Res, 4700 ohms, same as A21R20		
A21R26	Res, 100 k ohms, same as A21R4		

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A21R27	Res, 100 k ohms, same as A21R4		
A21R28	Res, 51 k ohms ±5%, 1/4 W, carbon	500 00513 00	2
A21R29	Res, 2000 ohms, same as A21R15		
A21R30	Res, 51 k ohms, same as A21R28		
A21R31	Res, 430 ohms ±5%, 1/4 W, carbon	500 00431 00	1
A21R32	Res, 10 k ohms, same as A21R1		
A21R33	Res, 2000 ohms, same as A21R15		
A21R34	Res, selected and installed during test Serial Nos. 101-200 only	500 series	1
A21R34	Res, 1000 ohms, same as A21R2 Serial Nos. 201 up		
A21R35	Res, 47 k ohms, same as A21R21		
A21R36	Res, 470 ohms ±5%, 1/4 W, carbon	500 00471 00	2
A21R37	Res, 470 ohms, same as A21R36		
A21R38	Res, 4300 ohms ±5%, 1/4 W, carbon	500 00432 00	1
A21R39	Res, 10 k ohms, same as A21R1		
A21R40	Res, var. 1 Meg ohm ±10%, 1/2 W, cermet	542 00003 10	1
A21R41	Res, 390 ohms ±5%, 1/4 W, carbon	500 00391 00	1
A21R42	Res, selected and installed during test	500 series	1
A21R43	Res, 110 ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00111 00	1
A21R44	Res, 1000 ohms, same as A21R2 Serial Nos. 201 up		
A21R45	Res, 2400 ohms ±5%, 1/4 W, carbon Serial Nos. 201 up	500 00242 00	1
A21R46	Res, var. 2000 ohms ±10%, 1/2 W, cermet Serial Nos. 201 up	542 00003 02	1
A21R47	Res, selected and installed during test As required for C-MSG		
	LEVEL COUNTER/AUTO OFF ASSEMBLY A22		
A22	Circuit Card Assembly, Level Counter/Auto Off	110 00147 00	1
A22C1	Cap, 22 μF (+50, −10%), 35 wvdc, elect'c	630 00004 00	2
A22C2	Cap, 22 μF, same as A22C1		
A22C3	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	3
A22C4	Cap, 10 μF, same as A22C3		
A22C5	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	4
A22C6	Cap, 10 μF, same as A22C3		
A22C7	Cap, 0.1 μF, same as A22C5		
A22C8	Cap, 0.1 μF, same as A22C5		
A22C9	Cap, 0.1 μF, same as A22C5		
A22CR1	Diode, type 1N914A	410 00015 00	5
A22CR2	Diode, 1N914A, same as A22CR1		
A22CR3	Diode, 1N914A, same as A22CR1		
A22CR4	Diode, 1N914A, same as A22CR1		
A22CR5	Diode, 1N914A, same as A22CR1		
A22I1	Integrated Circuit, DIP, type 4029B	430 00063 10	3
A22I2	Integrated Circuit, 4029B, same as A22I1		
A22I3	Integrated Circuit, 4029B, same as A22I1		
A22I4	Integrated Circuit, DIP, type 4013B	430 00048 10	1
A22I5	Integrated Circuit, DIP, type LM393N	431 00066 01	1
A22K1	Relay Latching 4A	705 00004 01	1
A22P1	Plug 26-pin Header Assy	812 00081 26	1
A22Q1	Transistor, silicon, NPN, type 2N5308	400 00025 00	1
A22R1	Res, 33 ohms ±5%, 1/4 W, carbon	500 00330 00	1
A22R2	Res, 150 k ohms ±5%, 1/4 W, carbon	500 00154 00	1
A22R3	Res, var, 20 k ohms ±10%, 1/2 W, cermet	542 00003 09	1
A22R4	Res, 43 k ohms ±5%, 1/4 W, carbon	500 00433 00	1
A22R5	Res, 20 k ohms ±5%, 1/4 W, carbon	500 00203 00	2

REF DES	DESCRIPTION	RYCOM NO.	QTY/ ASSY
A22R6	Res, 6800 ohms ±5%, 1/4 W, carbon	500 00682 00	1
A22R7	Res, 3000 ohms ±5%, 1/4 W, carbon	500 00302 00	1
A22R8	Res, 20 k ohms, same as A22R5		
A22R9	Res, 10 k ohms ±5%, 1/4 W, carbon	500 00103 00	1
A22R10	Res, 10 Meg ohms ±5%, 1/4 W, carbon	500 00106 00	1
	LEVEL DISPLAY ASSEMBLY A23		
A23	Circuit Card Assembly, Level Display	110 00148 00	1
A23C1	Cap, 200 pF ±5%, 100 wvdc, mica	610 20200 21	1
A23C2	Cap, 10 μF ±20%, 15 wvdc, tantalum	640 00001 01	2
A23C3	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	2
A23C4	Cap, 10 μF, same as A23C2		
A23C5	Cap, 0.1 μF, same as A23C3		
A23CR1	Diode, LED red	410 00044 00	1
A23CR2	Diode, LED yellow	410 00044 01	1
A23DH1	Heater, LCD	440 00003 01	1
A23I1	Integrated Circuit, type 4030B	430 00052 10	1
A23I2	Integrated Circuit, type 4543B	430 00072 10	3
A23I3	Integrated Circuit, 4543B, same as A23I2		
A23I4	Integrated Circuit, 4543B, same as A23I2		
A23I5	Integrated Circuit, 3.5 digit LCD	430 00105 00	1
A23J1	Connector Assy receptacle 26-pin	813 00022 26	1
A23R1	Res, 15 k ohms ±5%, 1/4 W, carbon	500 00153 00	1
	NOISE COMPENSATION ASSEMBLY A24		
A24	Circuit Card Assembly, Noise Compensation Serial Nos. 101-200 only	110 00151 00	1
A24	Circuit Card Assembly, Noise Compensation Serial Nos. 201 up	110 00151 01	1
A24R1	Res, var. 100 K ohm ±10%, 1/2 W, cermet	542 00003 11	3
A24R2	Res, var. 100 K ohm, same as A24R1		
A24R3	Res, var. 20 K ohm ±10%, 1/2 W, cermet	542 00003 09	1
A24R4	Res, var. 100 K ohm, same as A24R1		
A24R5	Res, var. 10 K ohm ±10%, 1/2 W, cermet	542 00003 05	1
A24R6	Res, var. 5 K ohm ±10%, 1/2 W, cermet	542 00003 03	1
A24R7	Res, 4700 ohm ±5%, 1/2 W, carbon Not Used on Serial Nos. 101-200	500 00472 00	1
A24	Circuit Card Assy, Noise Compensation, C-MSG	110 00151 02	1
A24R1	NOT USED		
A24R2	NOT USED		
A24R3	Res, var. 20 K ohm ±10%, 1/2 W, cermet	542 00003 09	2
A24R4	NOT USED		
A24R5	Res, var. 20 K ohm, same as A24R3		
A24R6	Res, var. 10 K ohm ±10%, 1/2 W, cermet	542 00003 05	1
A24R7	NOT USED		
	AFC LOWPASS FILTER ASSEMBLY A25		
A25	Circuit Card Assembly, AFC Lowpass Filter	110 00153 00	1
A25C1	Cap, 0.1 μF ±10%, 50 wvdc, mono	600 00015 01	4
A25C2	Cap, 0.1 μF, same as A25C1		
A25C3	Cap, 0.1 μF, same as A25C1		
A25C4	Cap, 0.1 μF, same as A25C1		
A25I1	Integrated Circuit, type 358N	431 00054 00	1
A25R1	Res, 470 k ohms ±5%, 1/4 W, carbon	500 00474 00	1
A25R2	Res, 240 k ohms ±5%, 1/4 W, carbon	500 00244 00	1
A25R3	Res, 160 k ohms ±5%, 1/4 W, carbon	500 00164 00	1

CHAPTER 10
COMPONENT LAYOUTS

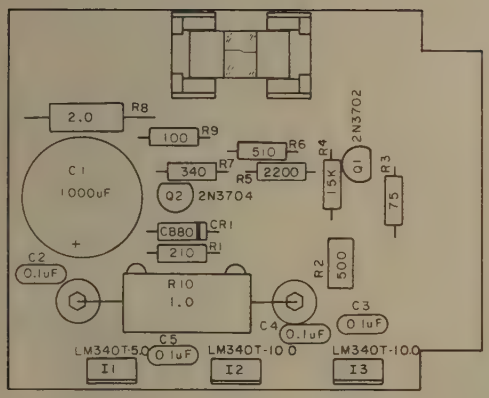


FIGURE 10-1a
POWER SUPPLY A1 (SERIAL NOS. 101-200)

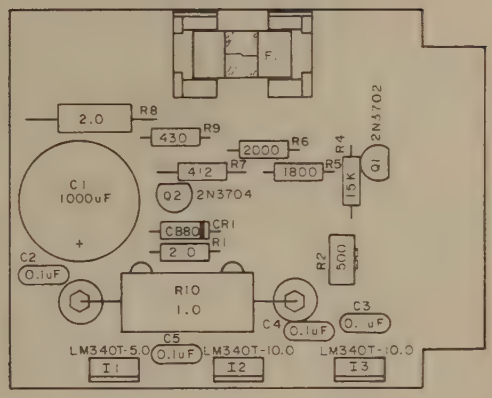
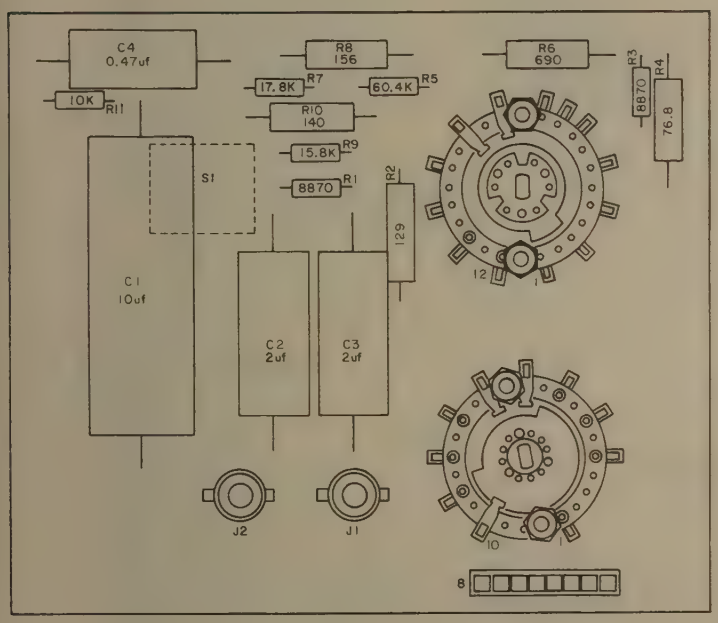
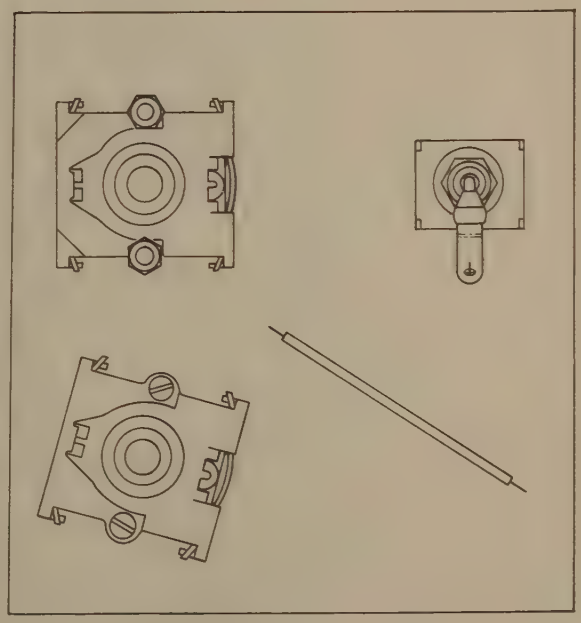


FIGURE 10-1b
POWER SUPPLY A1 (SERIAL NOS. 201 UP)

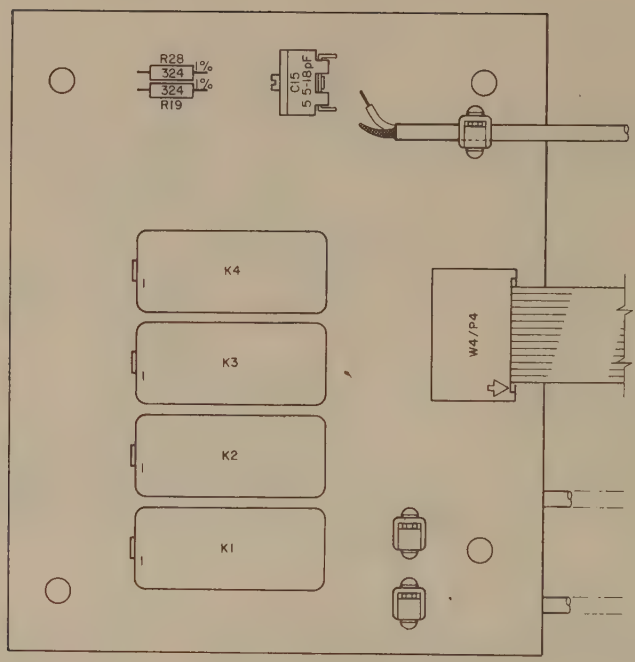


COMPONENT SIDE

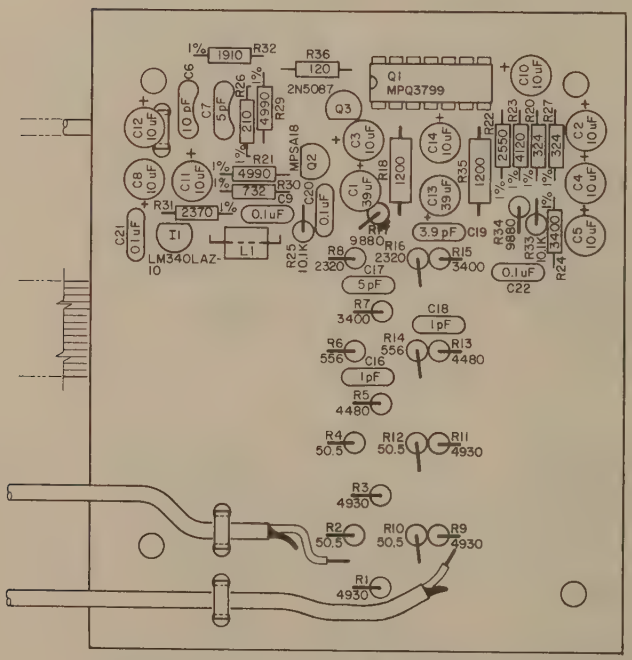


NON-COMPONENT SIDE

FIGURE 10-2
INPUT SELECTOR A2



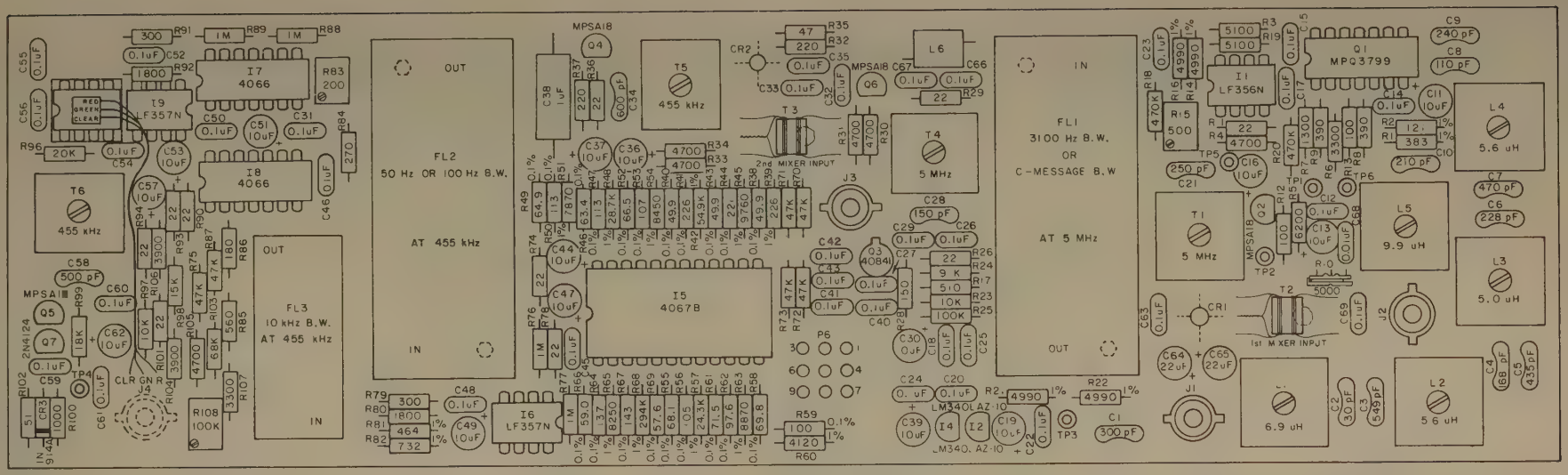
NON-COMPONENT SIDE



COMPONENT SIDE

Q1 (MPQ3799) MAY BE REPLACED BY 4 DISCRETE 2N3799 TRANSISTORS

FIGURE 10-3
ATTENUATOR/SUMMING AMPLIFIER A3



Q1 (MPQ3799) MAY BE REPLACED BY 3 DISCRETE 2N3799 TRANSISTORS
TEST POINTS TP5 AND TP6 ARE NOT ON SERIAL NOS. 101-200
R108 REPLACED 2 TEST SELECTED RESISTORS ON SERIAL NOS. 26 UP

FIGURE 10-4
I.F. A4

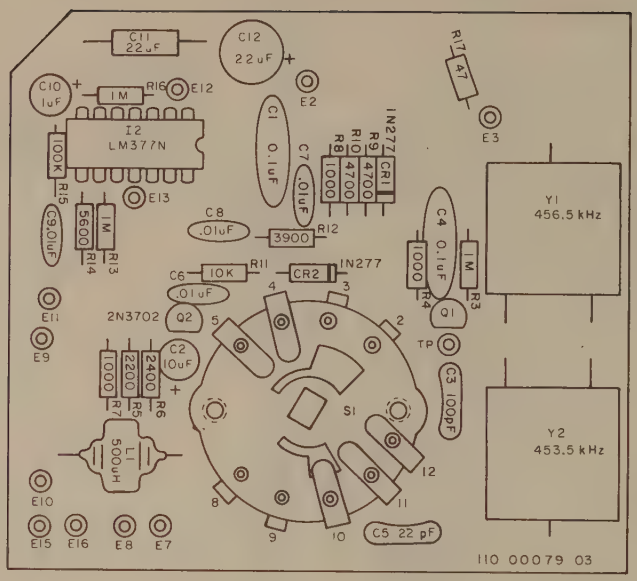


FIGURE 10-5
MONITOR A5

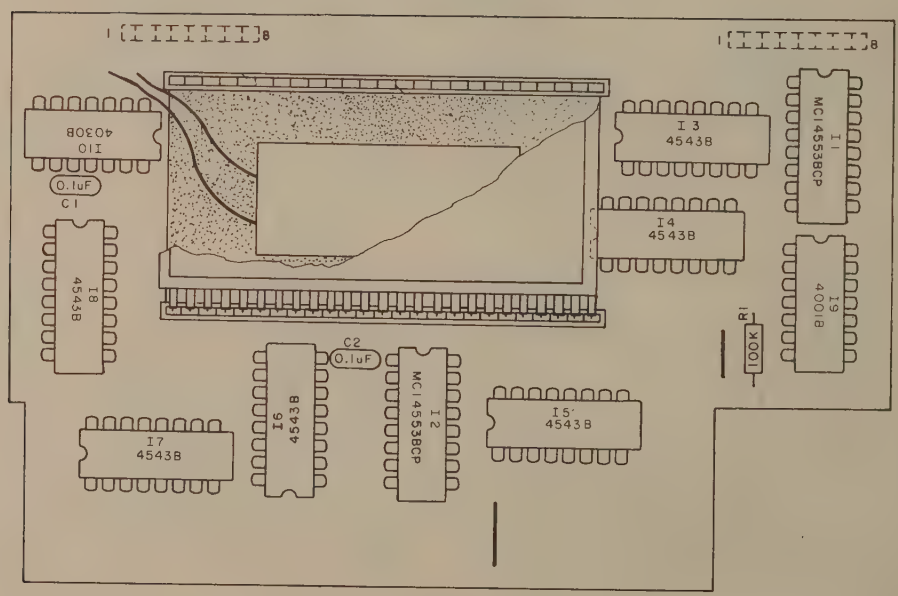
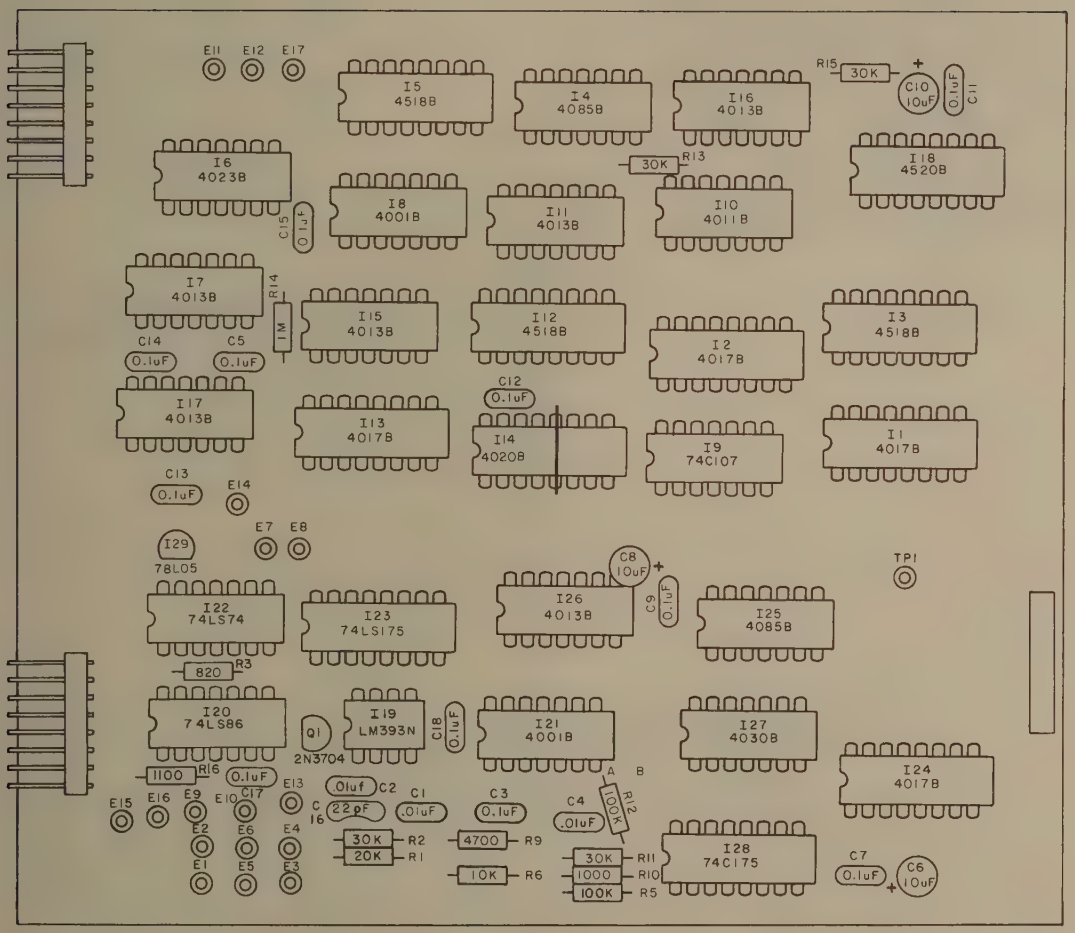
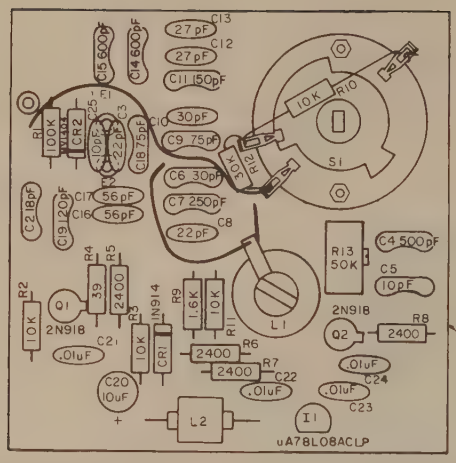


FIGURE 10-6
FREQUENCY DISPLAY A7



INTEGRATED CIRCUIT I9 IS A 74C73 ON SERIAL NOS. 101-200

FIGURE 10-7
TIMING/COUNTER INPUT A8



RESISTORS R9 AND R10 USAGE AND VALUE MAY VARY

FIGURE 10-8
1ST L.O. A9

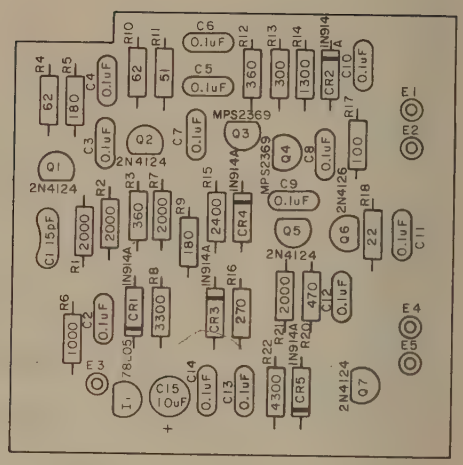
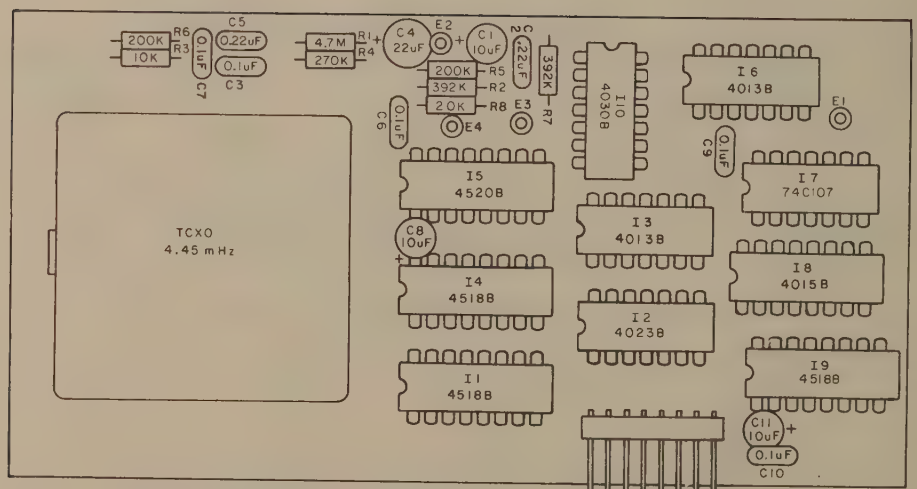


FIGURE 10-9
1ST L.O BUFFER/AMPLIFIER A10



INTEGRATED CIRCUIT I7 IS A 74C73 ON SERIAL NOS. 101-200

FIGURE 10-10
PHASE LOCK LOOPS A11

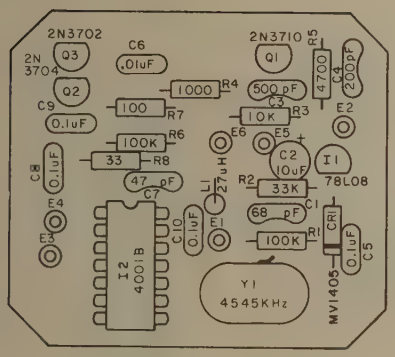


FIGURE 10-11
2ND L.O. A12

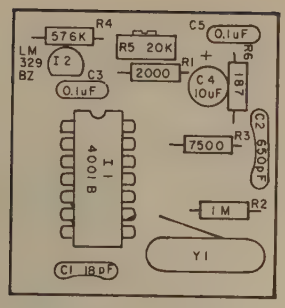


FIGURE 10-12
CALIBRATION OSCILLATOR A14

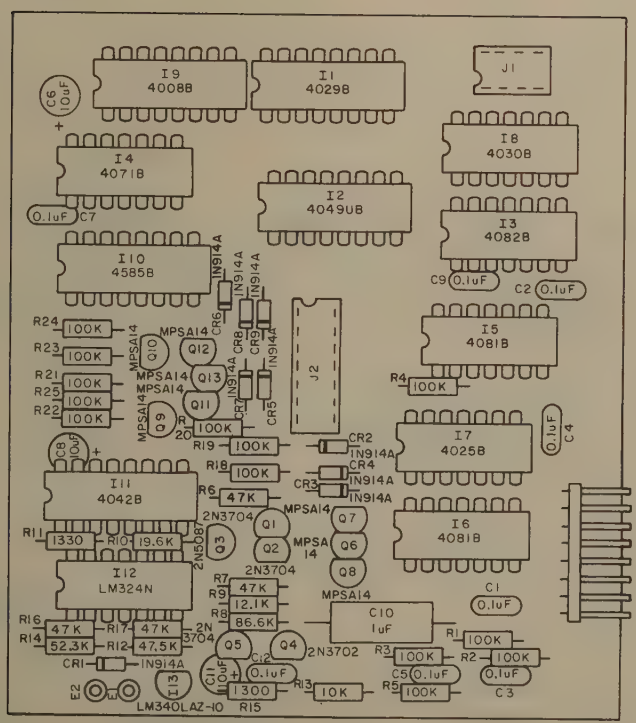


FIGURE 10-13
AUTO RANGING A19

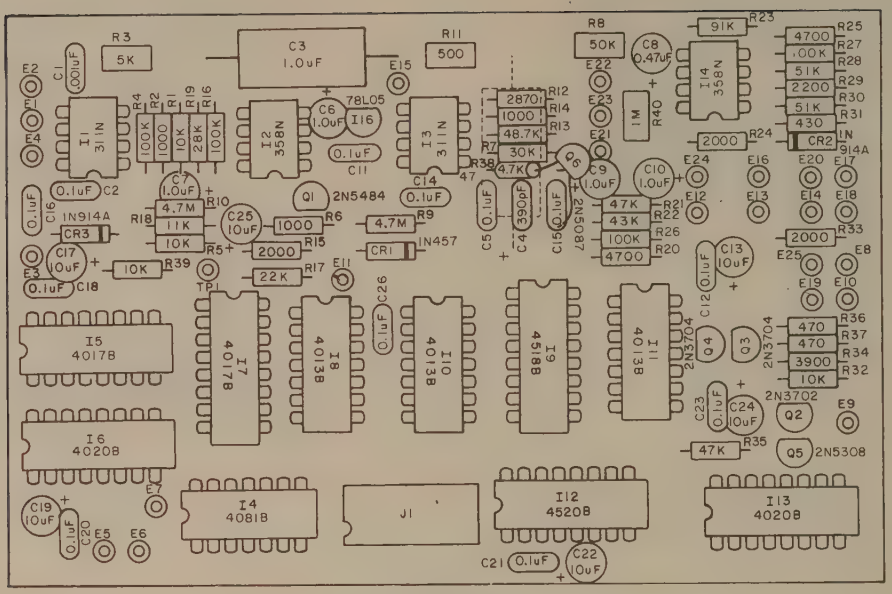


FIGURE 10-14a
LEVEL DETECTOR A21 (SERIAL NOS. 101-200)

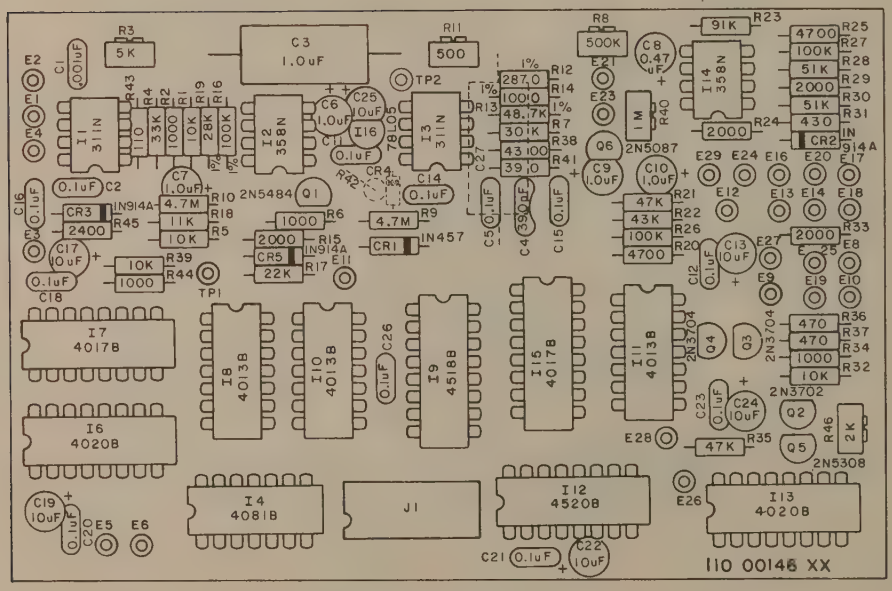


FIGURE 10-14b
LEVEL DETECTOR A21 (SERIAL NOS. 201 UP)

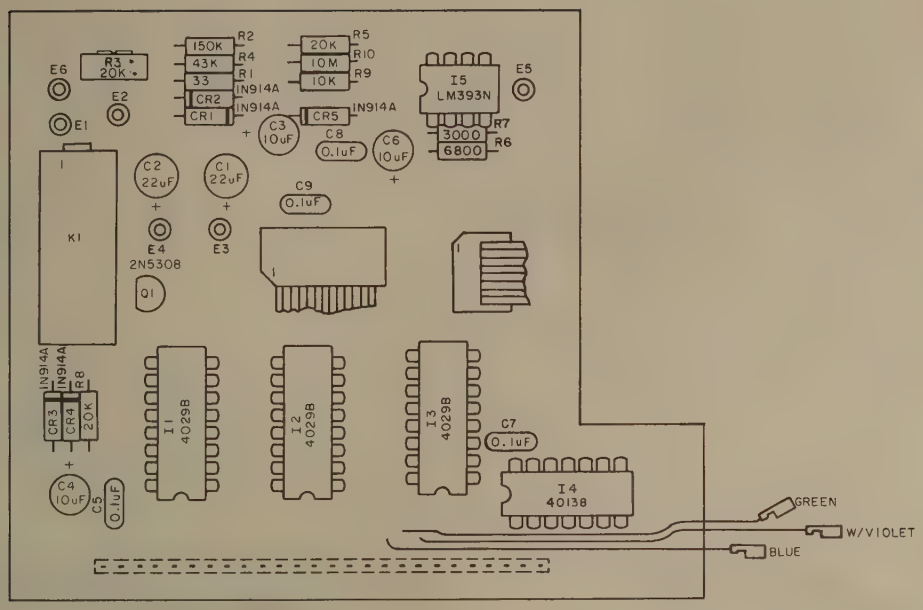


FIGURE 10-15
LEVEL COUNTER/AUTO OFF A22

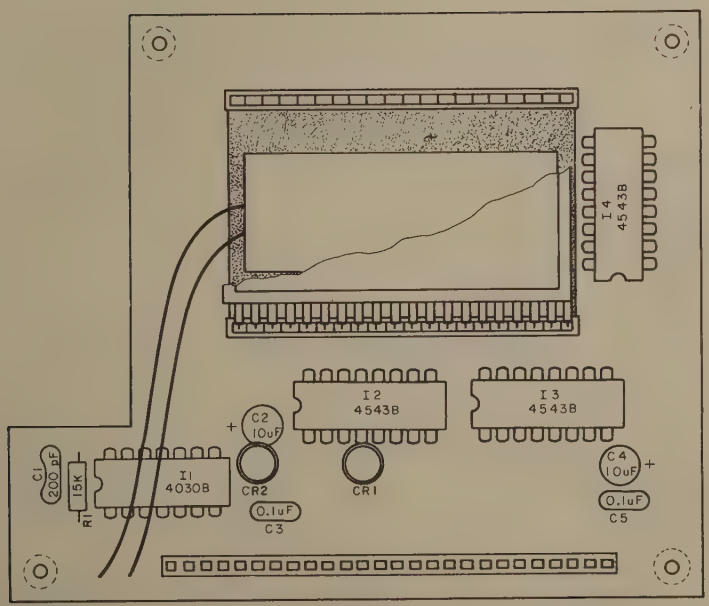


FIGURE 10-16
LEVEL DISPLAY A23

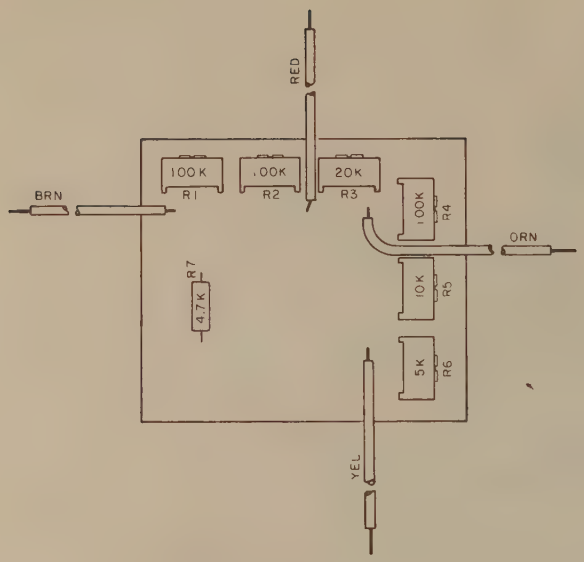


FIGURE 10-17a
NOISE COMPENSATION A24

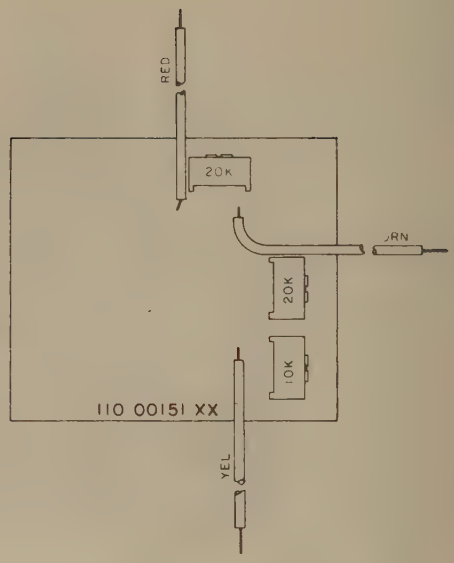


FIGURE 10-17b
NOISE COMPENSATION A24 (C-MSG)

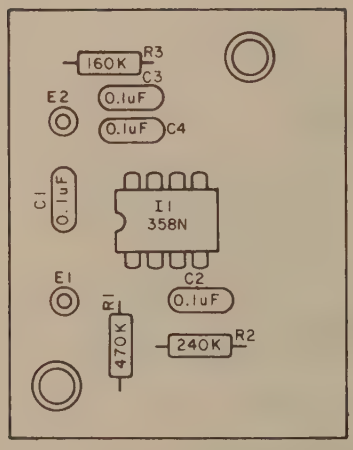


FIGURE 10-18
AFC LOWPASS FILTER A25

CHAPTER 11
CIRCUIT ELEMENTS

11.0 DIGITAL INTEGRATED CIRCUIT DESCRIPTION

The following is a functional description of the digital integrated circuits used throughout the 6040. These descriptions are provided as an aid in the trouble shooting of the various circuit boards. CMOS circuits are discussed first, followed by a discussion of Low Power Schottky TTL circuits.

11.0.1 4000 SERIES NOR-GATES

A positive logic NOR-gate will only have a hi output when all inputs are lo. Any hi input forces a lo output.

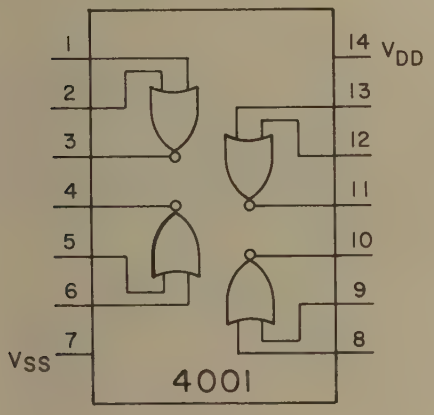


FIGURE 11-1a

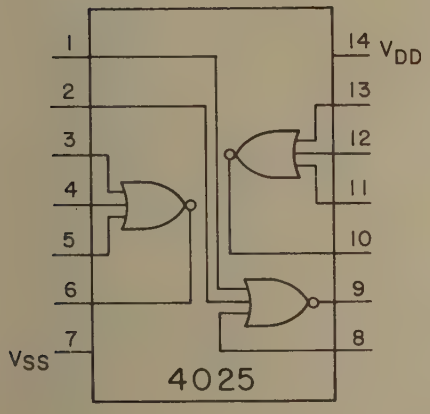


FIGURE 11-1b

11.0.2 4008 4-BIT FULL ADDER

The 4008 generates the sum of two 4-bit binary numbers. Inputs include the 4-bit sets of bits to be added, A1 to A4 and B1 to B4 and a "carry in" bit. Outputs include the four sum bits, S1 to S4 and a "carry out".

TRUTH TABLE				
C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1
0 = LO 1 = HI				

FIGURE 11-2a

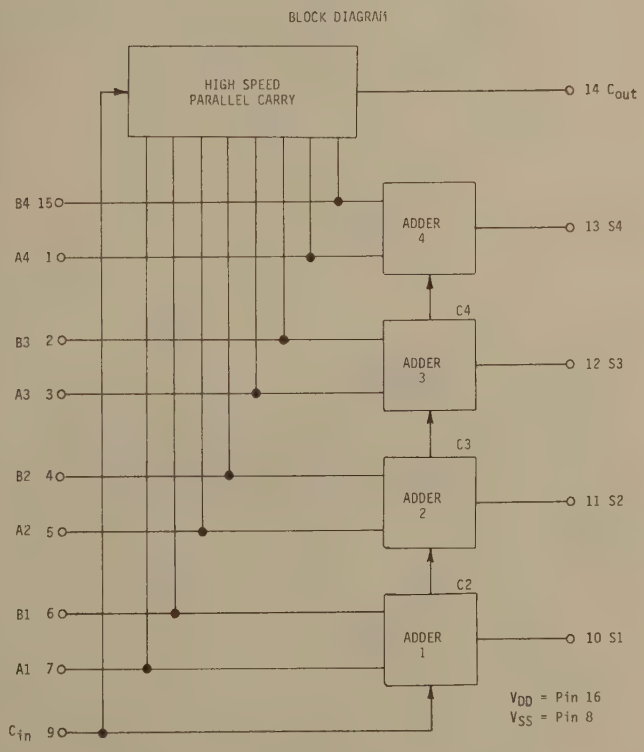


FIGURE 11-2b

11.0.3 4000 SERIES NAND-GATES

A positive logic NAND-gate will only have a lo output when all inputs are hi. Any lo input forces a hi output.

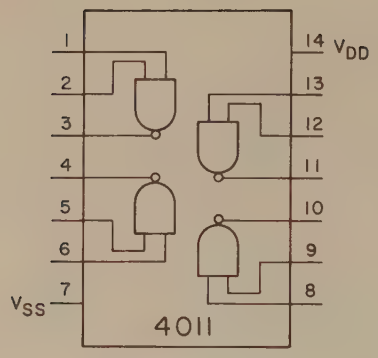


FIGURE 11-3a

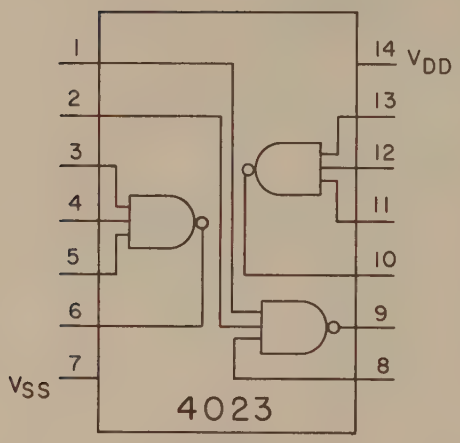


FIGURE 11-3b

11.0.4 4013 D FLIP-FLOP

The 4013 is an edge triggered Flip-Flop which is clocked by a rise of the signal at the clock input. Following a clock input and assuming lo state set and reset (clear) inputs, the Q output will be equal to the D input at the time of the clocking. A hi set input forces a hi Q output and a hi reset (clear) input forces a hi $\bar{Q}$ output.

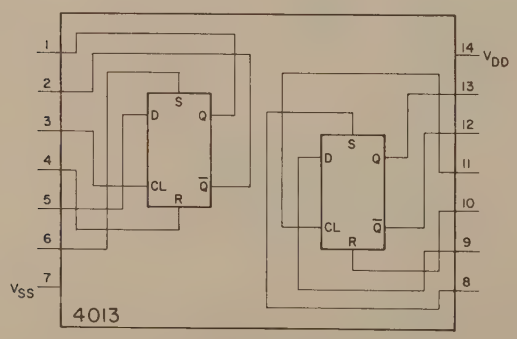


FIGURE 11-4a

4013 TRUTH TABLE					
CL	D	R	S	Q	$\bar{Q}$
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	X	0	0	NO CHANGE	
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

X = DON'T CARE
0 = LO
1 = HI

FIGURE 11-4b

11.0.5 4015 DUAL SHIFT REGISTER

The 4015 consists of two four-bit serial shift registers with parallel outputs. The registers respond to the rising edge of the clock signal. On each clock signal the output of a particular flip-flop is shifted to the succeeding flip-flop (Q1 to Q2 etc). The first flip-flop accepts the data input to be presented at the Q1 output. A hi reset input clears all the flip-flops of a register forcing all Q outputs to a lo state.

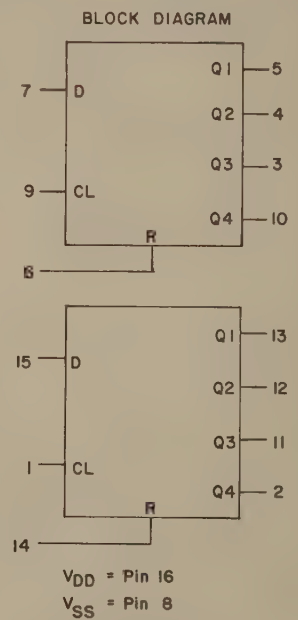


FIGURE 11-5a

TRUTH TABLE				
CL▲	D	R	Q1	Q_n
↗	0	0	0	Q_{n-1}
↗	1	0	1	Q_{n-1}
↘	X	0	Q1	Q_n (No change)
X	X	1	0	0

▲ Level change
X Don't care case

FIGURE 11-5b

11.0.6 4017 DECADE COUNTER

This decade counter has ten decoded outputs, one of which is hi for each count. The unit also has a carry output which is hi for counts 0-4. A hi reset input places the counter in a 0 count state. The unit counts when the Count Enable input is lo and a rise of the count input occurs or, when the Count Enable input is hi and a fall of the Count Enable occurs.

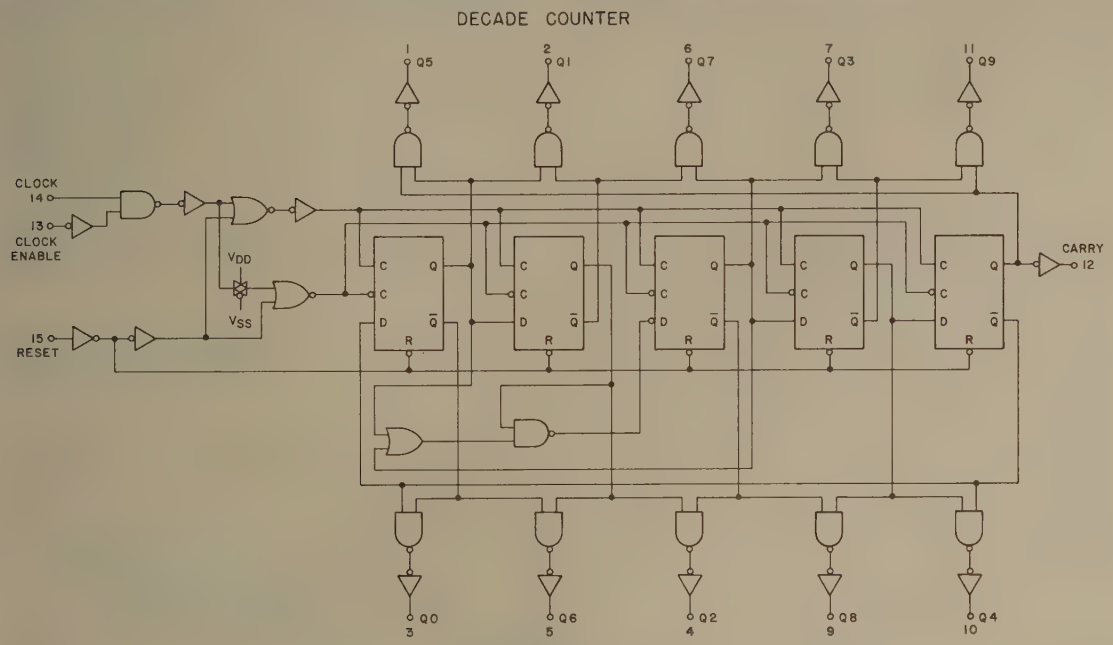


FIGURE 11-6a

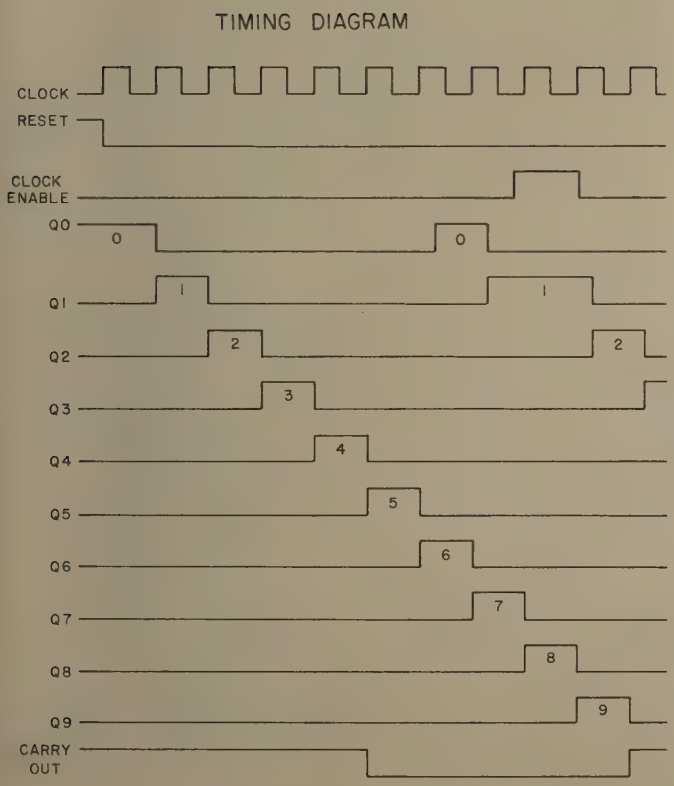


FIGURE 11-6b

TRUTH TABLE

CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
↗	0	0	n+1
↘	X	0	n
X	↗	0	n
1	↘	0	n+1

X = Don't care If n < 5 Carry = "1", Otherwise = "0"

FIGURE 11-6c

11.0.7 4020 14 STAGE RIPPLE COUNTER

This counter consists of 14 ripple-carry binary counter stages. The counter is reset to its "all zeros" state by a hi on the reset input. The counter is advanced one count on the negative-going transition of each input pulse. A binary up count takes place as each stage changes state; each time the preceding stages goes from a hi to lo output state.

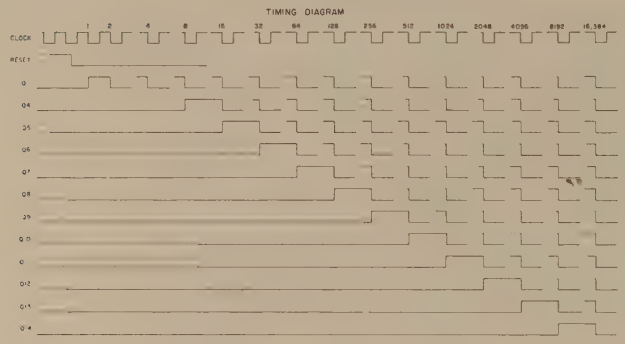


FIGURE 11-7a

TRUTH TABLE

$\overline{\text{CLOCK}}$	RESET	OUTPUT STATE
⌐	0	NO CHANGE
¬	0	ADVANCE TO NEXT STATE
X	1	ALL OUTPUTS ARE LOW

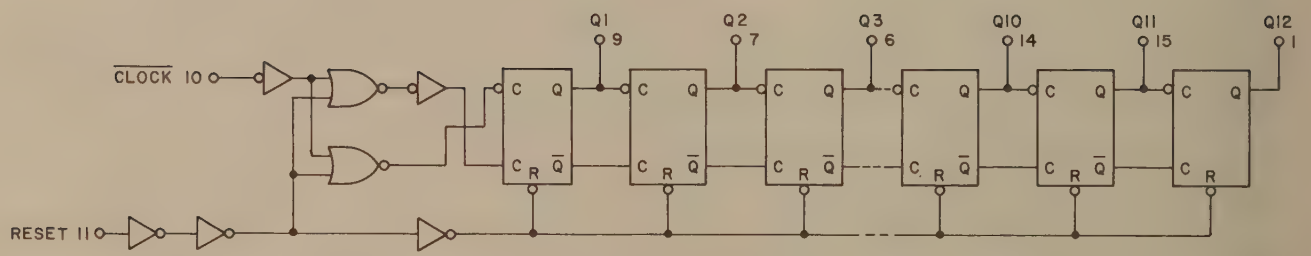
X = DON'T CARE
0 = LO
1 = HI

FIGURE 11-7C

11.0.8 4023 (see section 11.0.3)

11.0.9 4025 (see section 11.0.1)

LOGIC DIAGRAM



Q4 = PIN 5 Q7 = PIN 4
Q5 = PIN 3 Q8 = PIN 13
Q6 = PIN 2 Q9 = PIN 12

V_{DD} = PIN 16
V_{SS} = PIN 8

FIGURE 11-7b

11.0.10 4029 PRESETTABLE UP/DOWN COUNTER

The 4029 is a four stage counter which will count up with a hi Up/Down input and count down with a lo Up/Down input. A count change takes place when the "carry-in" input is lo and a rise occurs on the clock input. The counter is set to the count determined by the preset inputs (P1, P2, P3 and P4) when the preset enable (PE) input goes hi. A hi on the B/D input forces the counter to count in a binary mode while a lo B/D input forces the counter to count in a BCD mode.

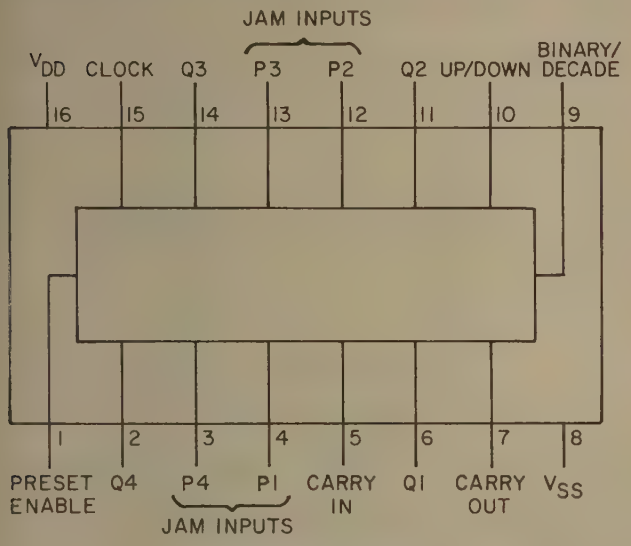


FIGURE 11-10a

TRUTH TABLE

$\overline{CI}$	U/D	PE	B/D	ACTION
1	X	0	X	NO COUNT
0	1	0	0	COUNT UP (DECADE)
0	1	0	1	COUNT UP (BINARY)
0	0	0	0	COUNT DOWN (DECADE)
0	0	0	1	COUNT DOWN (BINARY)
X	X	1	X	PRESET

X = DON'T CARE
TRANSITIONS OCCUR ON CLOCK RISE

FIGURE 11-10b

4029

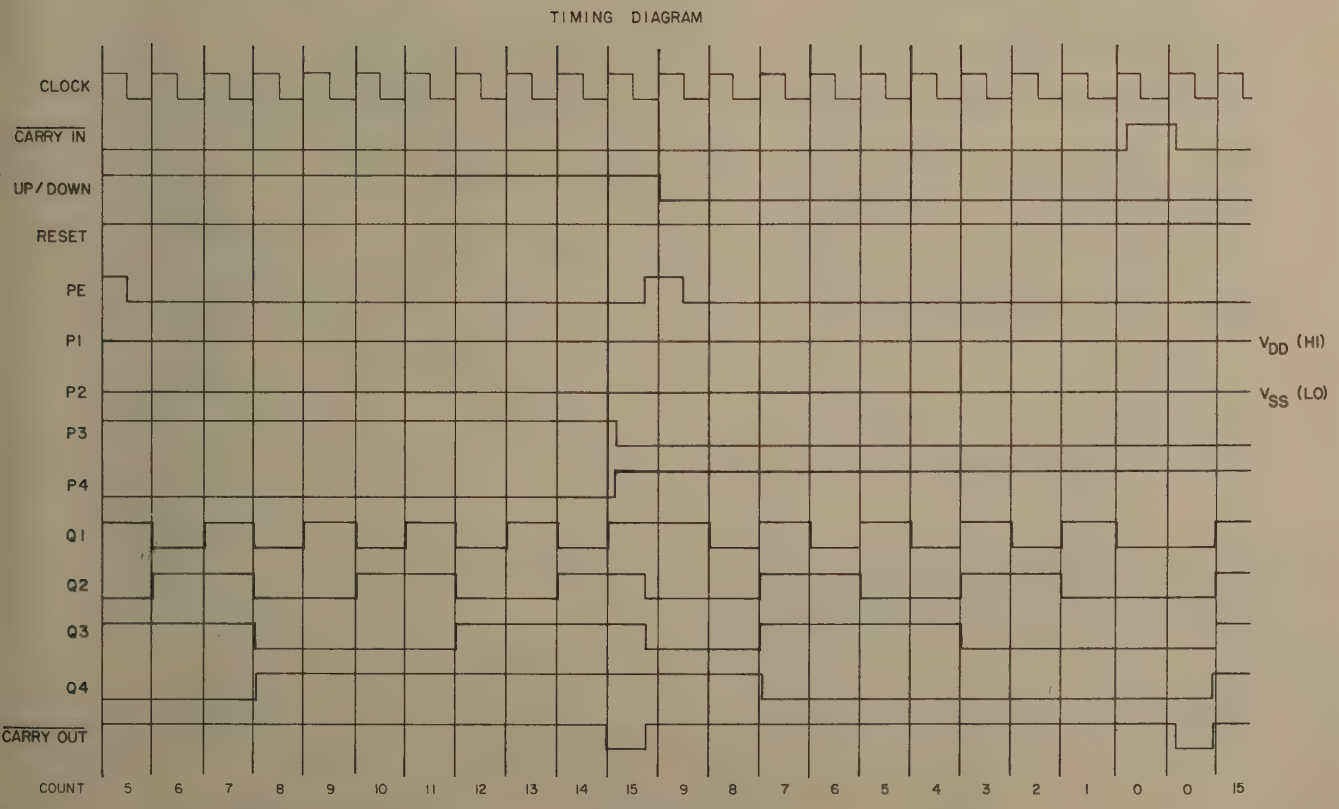


FIGURE 11-10c

11.0.11 4030 EXCLUSIVE-OR GATE

An EXCLUSIVE-OR gate is a two input device. The output will be hi only when there is a single hi input. In order to have a single hi input, the inputs must be different. The output will be lo when both inputs are the same.

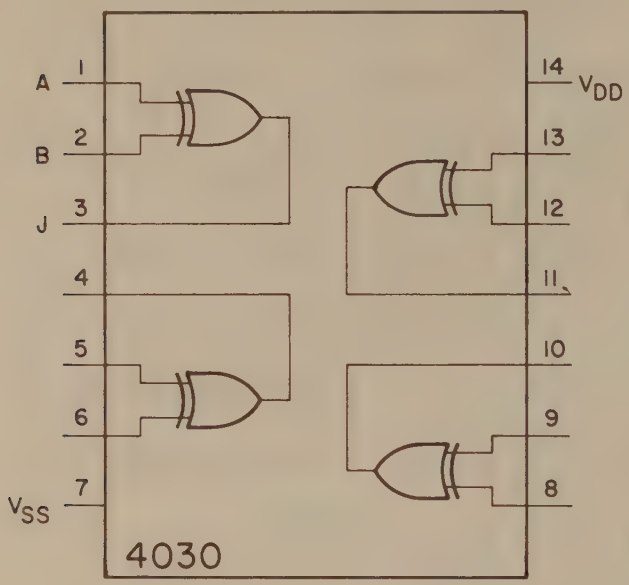


FIGURE 11-11a

4030 TRUTH TABLE		
A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

0 = LO
1 = HI

FIGURE 11-11b

11.0.12 4042 QUAD CLOCKED "D" LATCH

This quad latch contains four latch circuits, each strobed by a common clock. Complementary outputs are available from each circuit. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\bar{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "O" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

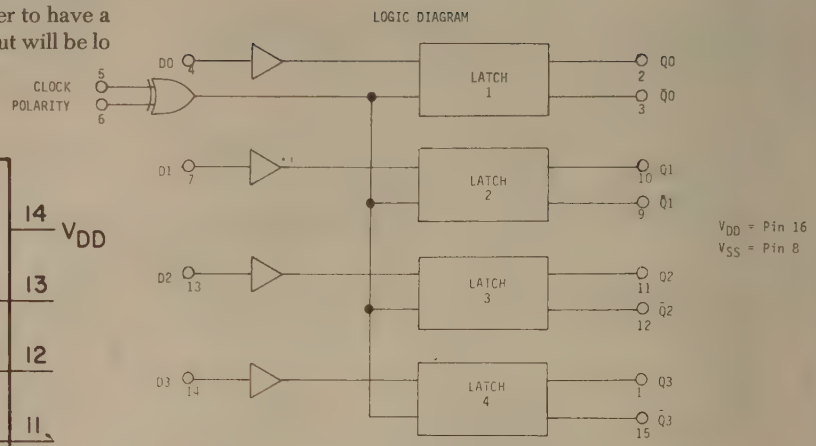


FIGURE 11-12a

TRUTH TABLE

CLOCK	POLARITY	Q
0	0	DATA
↗	0	LATCH
1	1	DATA
↘	1	LATCH

FIGURE 11-12b

11.0.13 4049 HEX BUFFER

The 4049 is a hex inverter/buffer. Each circuit converts a hi input to a lo output and converts a lo input to a hi output.

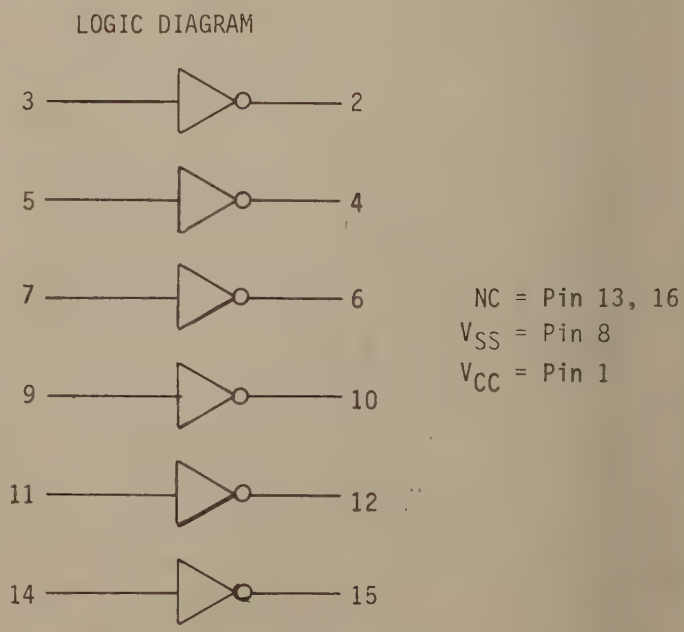


FIGURE 11-13a

11.0.14 4066 QUAD ANALOG SWITCH/QUAD MULTIPLEXER

This quad bilateral switch consists of four independent switches capable of controlling either digital or analog signals. A hi control input generates low impedance between the in/out and out/in terminals while a lo control input generates a high impedance between the two terminals.

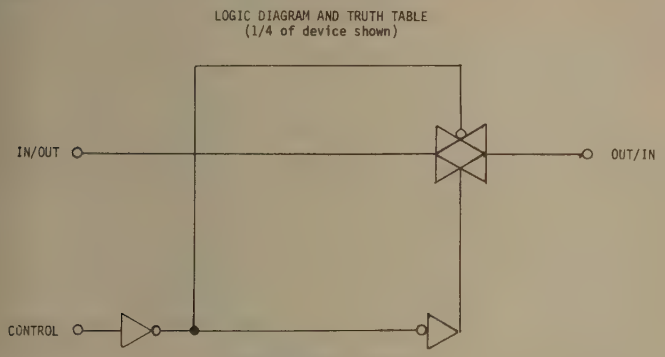


FIGURE 11-14a

CONTROL	SWITCH
0	OFF
1	ON

LOGIC DIAGRAM RESTRICTIONS

V_{SS} V_{IN} V_{DD}

V_{SS} V_{OUT} V_{DD}

$V_{CONTROL}$	V_{IN} TO V_{OUT} RESISTANCE
V_{SS}	10^9 OHMS TYP
V_{DD}	3×10^2 OHMS TYP

FIGURE 11-14b

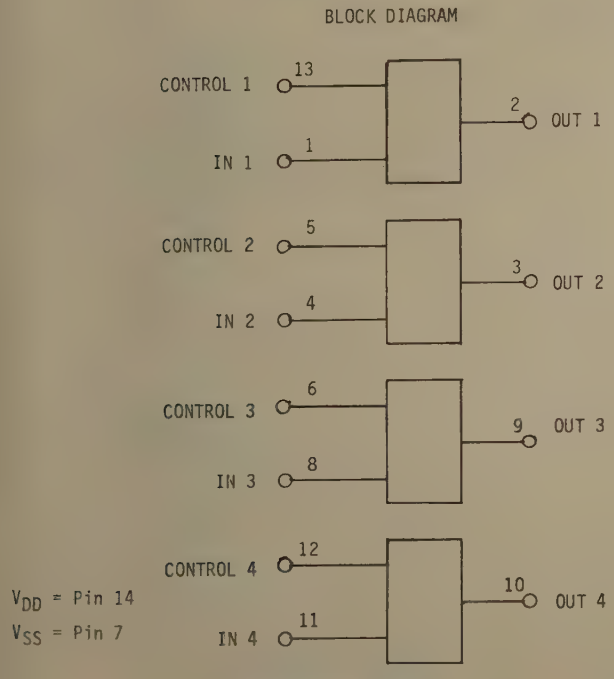


FIGURE 11-14c

11.0.15 4067 ANALOG MULTIPLEXER/DEMULTIPLEXER

The 4067 is a digitally controlled analog switch having low ON impedance, low OFF leakage current, and internal address decoding. It is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

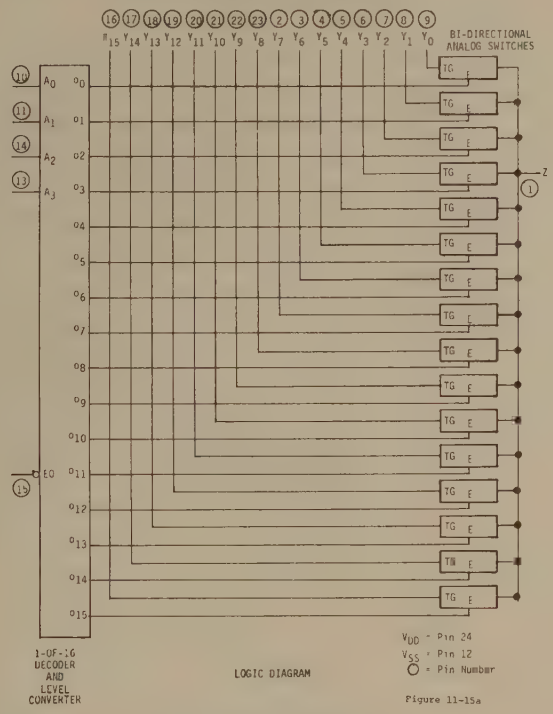


FIGURE 11-15a

TRUTH TABLE

A	B	C	D	INH	SELECTED CHANNEL
X	X	X	X	1	NONE
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	1	15

FIGURE 11-15b

11.0.16 4071 QUAD 2-INPUT "OR" GATE

A positive logic OR gate will have Hi output when any input is Hi. A Lo output is generated only when all inputs are Lo.

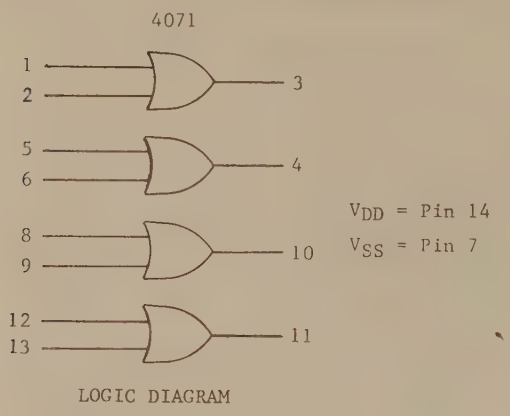


FIGURE 11-16a

11.0.17 4000 SERIES AND GATES

A positive logic AND gate will only have a Hi output when all inputs are Hi. Any low Lo input will generate a Lo output.

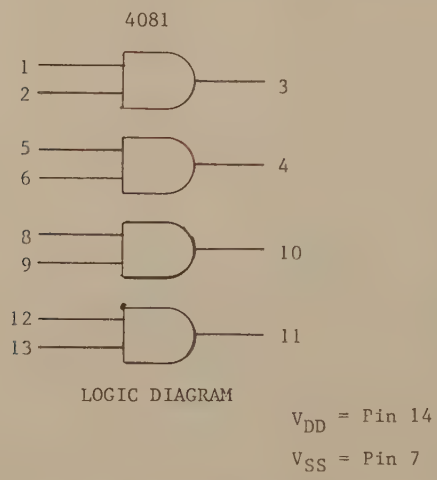


FIGURE 11-17a

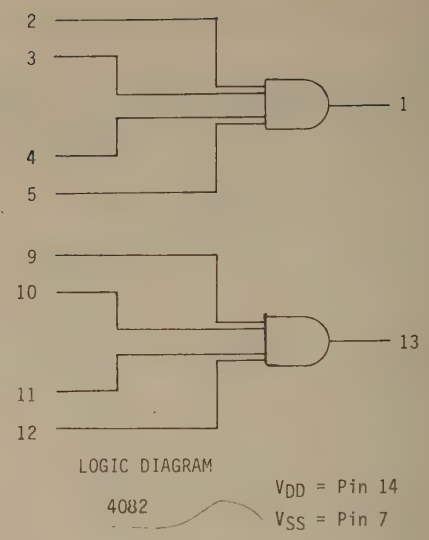


FIGURE 11-17b

11.0.18 4085 DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

The 4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. The 4085 also has individual inhibit controls. An output will be Lo anytime the inhibit input is Hi or any pair of AND gate inputs are both Hi. An output will be Hi only when the inhibit input is Lo and each AND gate has at least one Lo input.

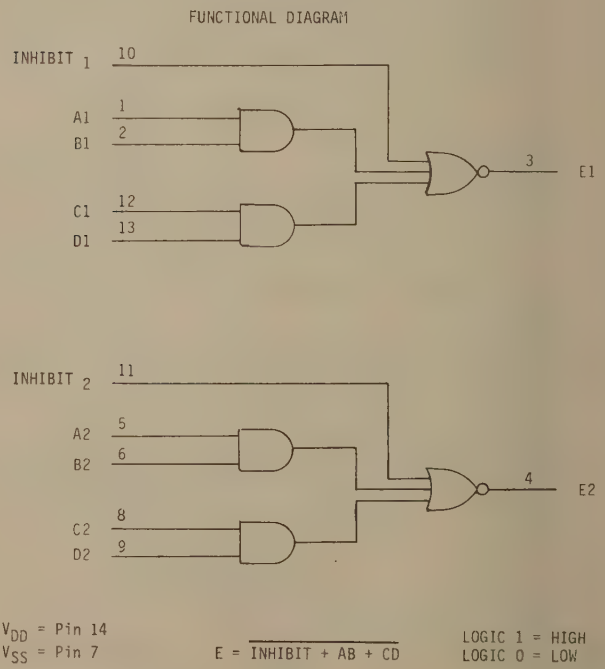


FIGURE 11-18a

11.0.19 4518 DUAL BCD UP COUNTER

The 4518 consists of two four-stage counters. These BCD counters will advance from a decimal 9 count in binary code to a 0 count. A count will be clocked when the clock input rises and the enable input is hi or when the enable input falls and the clock input is lo. A hi reset input forces the counter to 0 count output.

BLOCK DIAGRAM

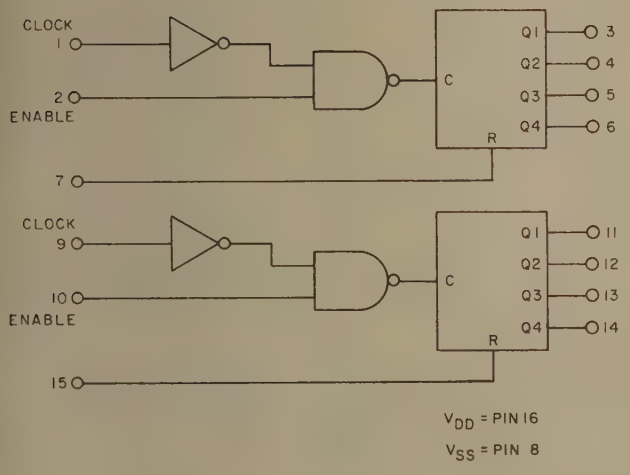


FIGURE 11-19a

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐‾	1	0	INCREMENT COUNTER
0	‾⌐	0	INCREMENT COUNTER
‾⌐	X	0	NO CHANGE
X	⌐‾	0	NO CHANGE
⌐‾	0	0	NO CHANGE
1	‾⌐	0	NO CHANGE
X	X	1	Q1 THRU Q4 = 0

X = DON'T CARE
0 = LO
1 = HI

FIGURE 11-19b

TIMING DIAGRAM

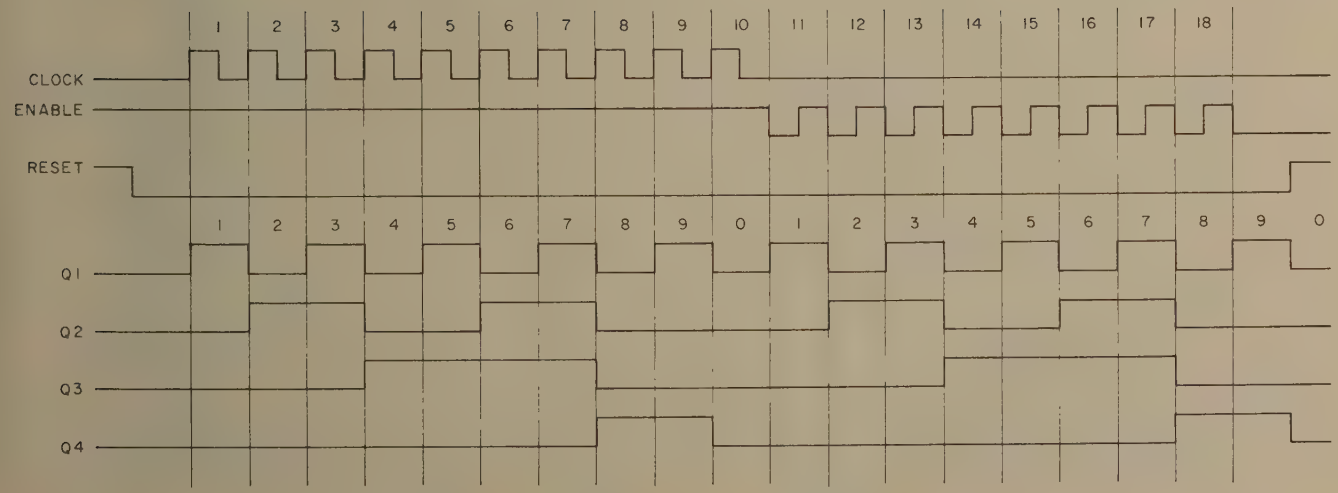
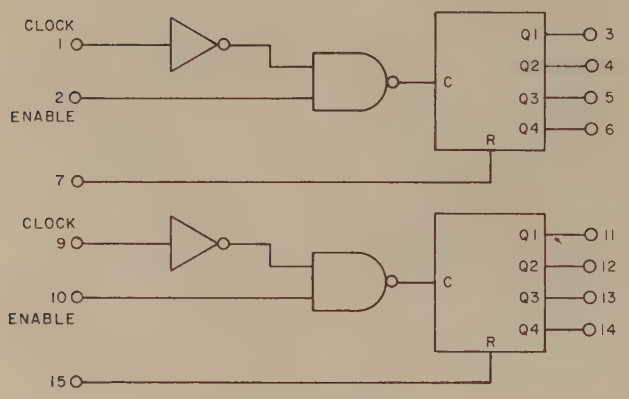


FIGURE 11-19c

11.0.20 4520 DUAL BINARY UP COUNTER

The 4520 consists of two four-stage binary counters. A count will be clocked when the clock input rises and the enable input is hi or when the enable input falls and the clock input is lo. A hi reset input forces the counter to a 0 count output.

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

FIGURE 11-20a

TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐	1	0	INCREMENT COUNTER
0	¬	0	INCREMENT COUNTER
¬	X	0	NO CHANGE
X	⌐	0	NO CHANGE
⌐	0	0	NO CHANGE
1	¬	0	NO CHANGE
X	X	1	Q1 THRU Q4 = 0

X = DON'T CARE
0 = LO
1 = HI

FIGURE 11-20b

TIMING DIAGRAM

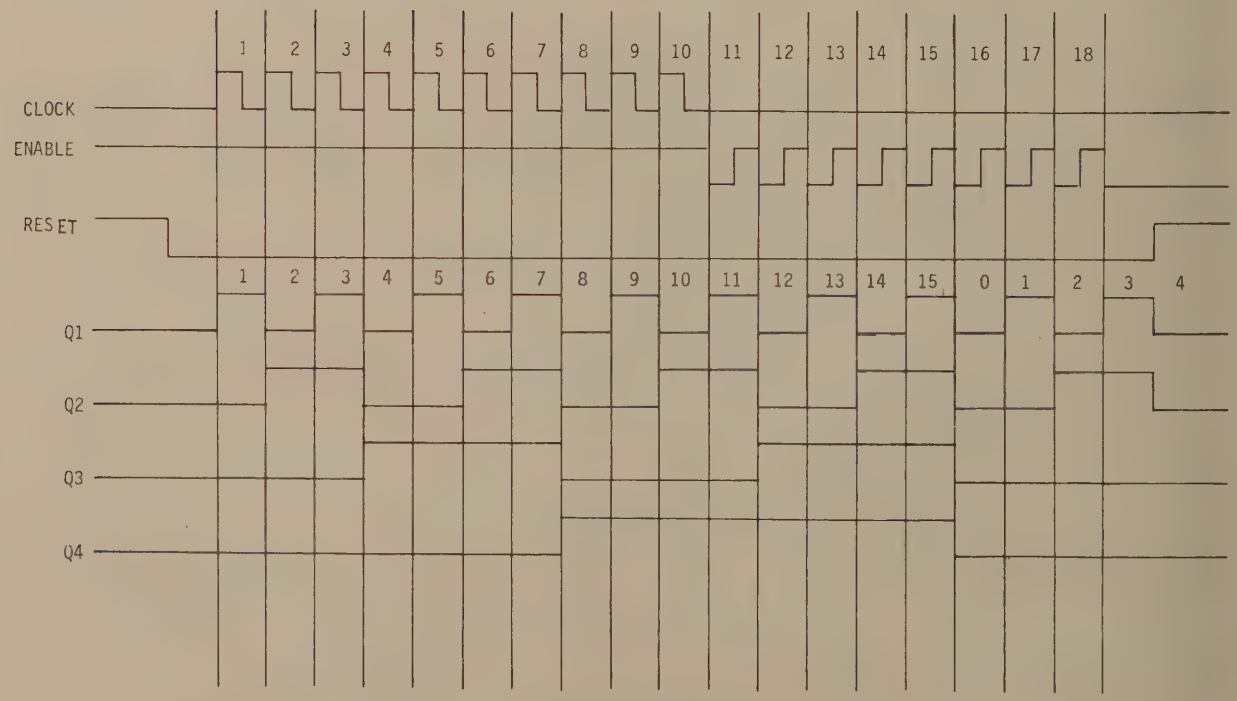
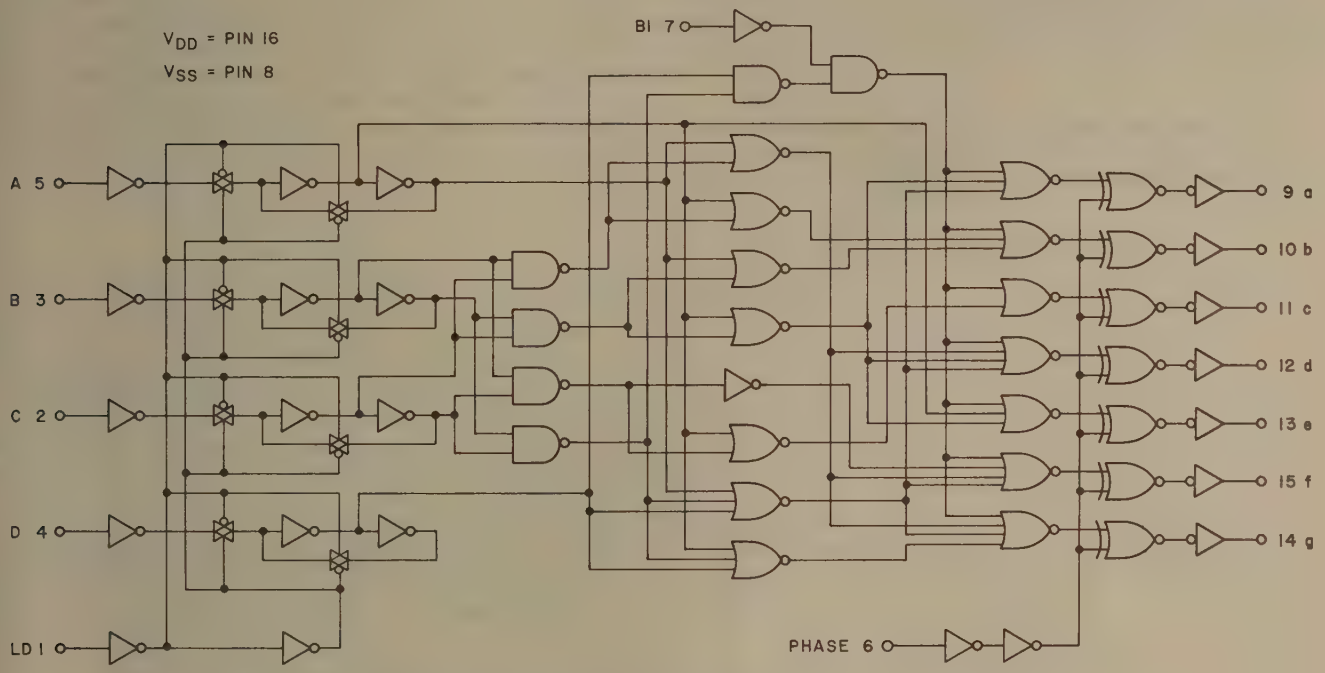


FIGURE 11-20c

11.0.21 4543 BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The BCD-to-seven segment latch/decoder/driver provides the functions of a 4-bit storage latch and an 8421 BCD-to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The phase (Ph), blanking (Bl), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively.

LOGIC DIAGRAM



4543 BCD TO SEVEN SEGMENT
LATCH/DECODER/DRIVER

FIGURE 11-21a

TRUTH TABLE

INPUTS							OUTPUTS							
LD	Bl	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.
0 = Lo
1 = Hi

FIGURE 11-21b

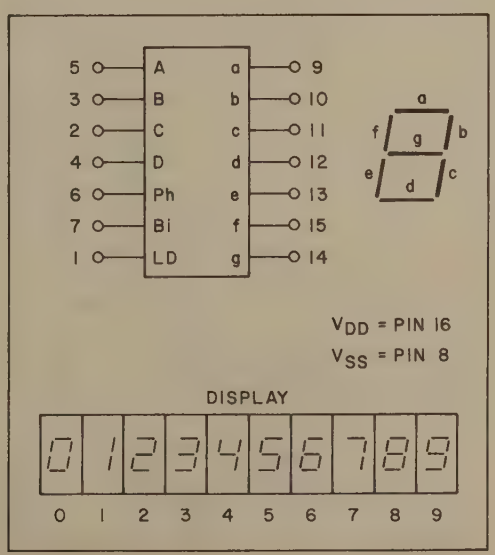


FIGURE 11-21c

11.0.22 4553 THREE DIGIT COUNTER

The three-digit counter consists of three negative edge-triggered BCD counters which are cascaded in a synchronous fashion. A quad latch at the output of each of the three BCD counters permits storage of any given count. The three sets of BCD outputs (active hi), after going through the latches, are time division multiplexed, providing one BCD number or digit at a time. Digit select outputs (active lo) are provided for display control.

An on-chip oscillator provides the low frequency scanning clock which drives the multiplexer output selector. The frequency of the oscillator can be controlled externally by a capacitor between pins 3 and 4 or it can be overridden and driven by an external clock at pin 4. Multiple devices can be cascaded using the overflow output, which provides one pulse for every 1000 counts.

A hi Master Reset initializes the three BCD counters and the multiplexer scanning circuit. While Master Reset is hi, the digit scanner is set to digit one; all three digit select outputs are disabled and the scan oscillator is inhibited. The Disable input, when hi, prevents the input clock from reaching the counters, while still retaining the last count. Information present in the counters when the latch input goes hi, will be stored in the latches and will be retained while the latch is hi, independent of other inputs. Information can be recovered from the latches after counters have been reset if Latch Enable remains hi during the entire reset cycle.

TRUTH TABLE

INPUTS				OUTPUTS
MASTER RESET	CLOCK	DISABLE	LE	
0	⌐	0	0	NO CHANGE
0	¬	0	0	ADVANCE
0	X	1	X	NO CHANGE
0	1	⌐	0	ADVANCE
0	1	¬	0	NO CHANGE
0	0	X	X	NO CHANGE
0	X	X	⌐	LATCHED
0	X	X	1	LATCHED
1	X	X	X	Q0=Q1=Q2=Q3=0

X = DON'T CARE

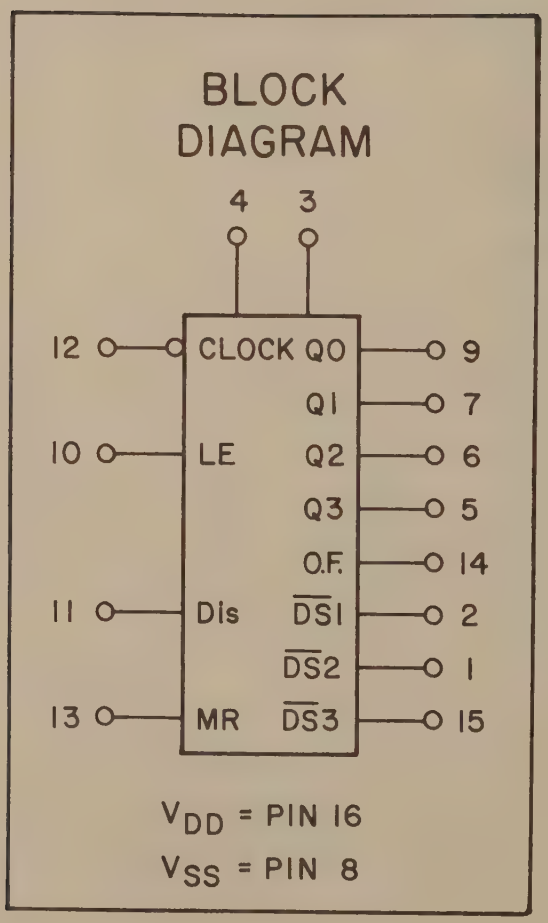


FIGURE 11-22a

FIGURE 11-22b

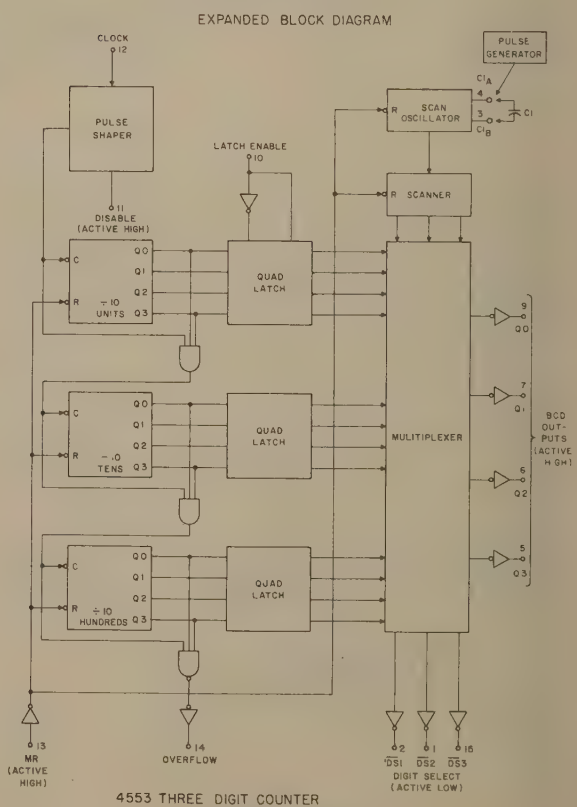


FIGURE 11-22c

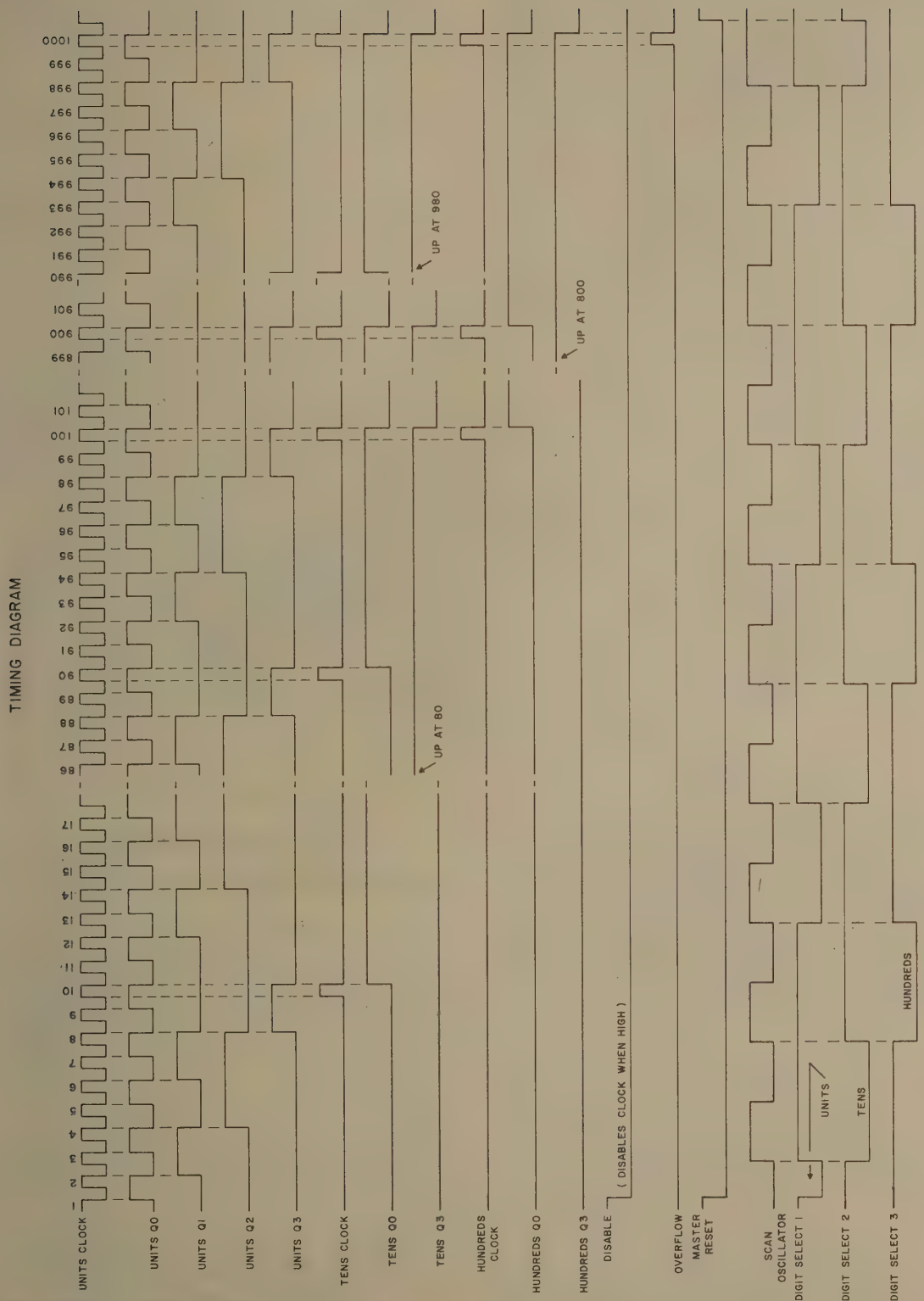


FIGURE 11-22d

11.0.23 4585 4-BIT MAGNITUDE COMPARATOR

The 4585 circuit has eight comparing inputs and three outputs. This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output.

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3,B3	A2,B2	A1,B1	A0,B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3 A3=B3 A3=B3 A3=B3	X A2>B2 A2=B2 A2=B2	X X A1>B1 A1=B1	X X X A0>B0	X X X X	X X X X	1 1 1 1	0 0 0 0	0 0 0 0	1 1 1 1
A3=B3 A3=B3 A3=B3	A2=B2 A2=B2 A2=B2	A1=B1 A1=B1 A1=B1	A0=B0 A0=B0 A0=B0	0 0 1	0 1 0	1 X X	0 0 1	0 1 0	1 0 0
A3=B3 A3=B3 A3=B3 A3<B3	A2=B2 A2=B2 A2<B2 X	A1=B1 A1<B1 X X	A0<B0 X X X	X X X X	X X X X	X X X X	1 1 1 1	0 0 0 0	0 0 0 0

X = DON'T CARE

FIGURE 11-23a

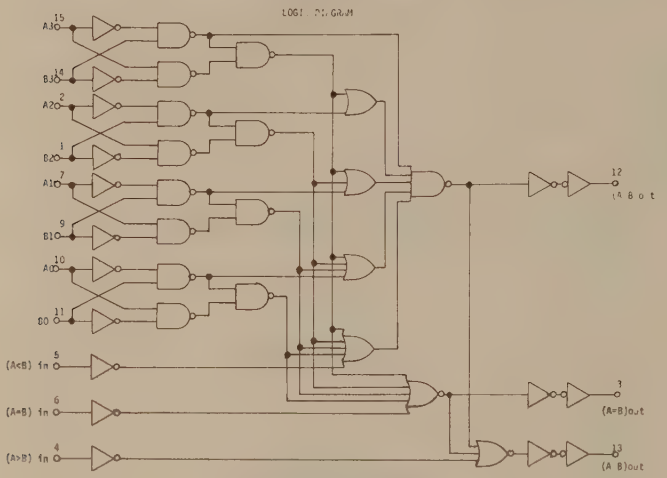


FIGURE 11-23b

11.0.24 74C SERIES JK FLIP-FLOPS

The 74C JK flip-flop is an edge triggered flip-flop that is clocked on the falling edge of the clock input. A clock fall will bring the Q output hi with a hi J and a low K input. A clock fall will bring the $\bar{Q}$ output hi with a hi K input and a lo J input. A clock fall will change the state of the flip-flop when both J and K inputs are hi. No change will take place when the clock falls when both J and K inputs are lo. A lo reset input forces a hi $\bar{Q}$ output and inhibits control by other inputs.

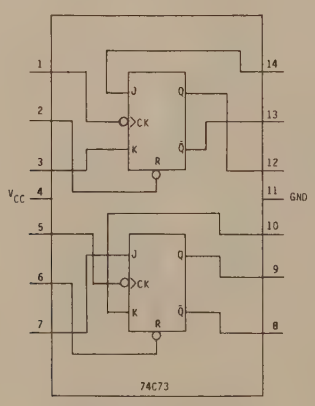


FIGURE 11-24a

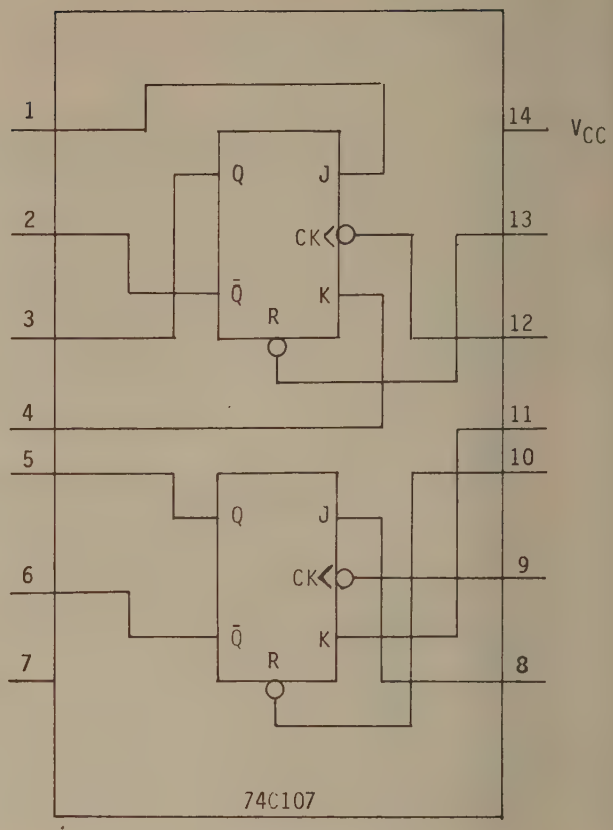


FIGURE 11-24b

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

0 = LO
1 = HI

t_n = BIT TIME BEFORE CLOCK PULSE.
t_{n+1} = BIT TIME AFTER CLOCK PULSE.

FIGURE 11-24c

11.0.25 74C175 QUAD D-TYPE FLIP-FLOP

The 74C175 contains four D-type flip-flops. The flip-flops transfer the data input to the Q output on the rise of the clock input signal. All four flip-flops share a common clock input. The flip-flops also share a common active lo reset input. A lo reset input will transfer and hold the flip-flops in a reset state (Q lo-$\bar{Q}$ hi).

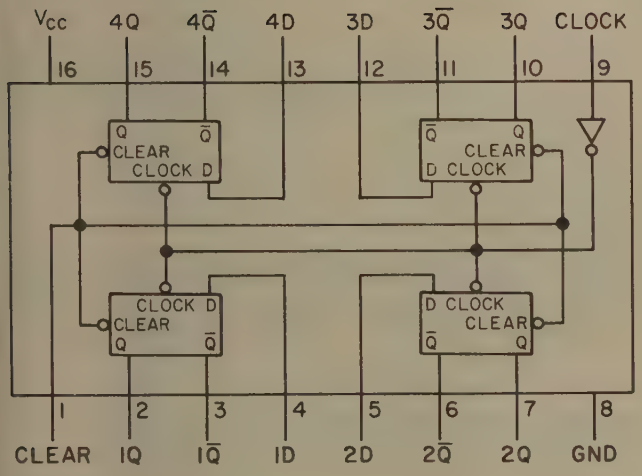

Vcc 4Q 4Q̄ 4D 3D 3Q̄ 3Q CLOCK
16 15 14 13 12 11 10 9
Q Q̄ CLEAR CLOCK D
Q̄ Q CLEAR D CLOCK
CLOCK D CLEAR Q Q̄
D CLOCK CLEAR Q̄ Q
1 2 3 4 5 6 7 8
CLEAR 1Q 1Q̄ 1D 2D 2Q̄ 2Q GND

FIGURE 11-25a

TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
0	X	X	0	1
1	⌐⌐	1	1	0
1	⌐⌐	0	0	1
1	1	X	NC	NC
1	0	X	NC	NC

1 = HIGH LEVEL
0 = LOW LEVEL
⌐⌐ = TRANSITION FROM LOW TO HIGH LEVEL
X = IRRELEVANT
NC = NO CHANGE

FIGURE 11-25b

11.0.26 74LS74 DUAL D TYPE FLIP-FLOP

The 74LS74 is a low power Schottky TTL D flip-flop. A TTL hi level may be +2.0 V to +5.0 V. A lo level will be less than 0.4 V. A D flip-flop is an edge triggered flip-flop which is clocked by a rise of the signal at the clock input. Following a clock input and assuming hi state set and reset (clear) inputs, the Q output will be equal to the D input at the time of the clocking. A lo set input forces a hi $\bar{Q}$ output and a lo reset (clear) input forces a hi output.

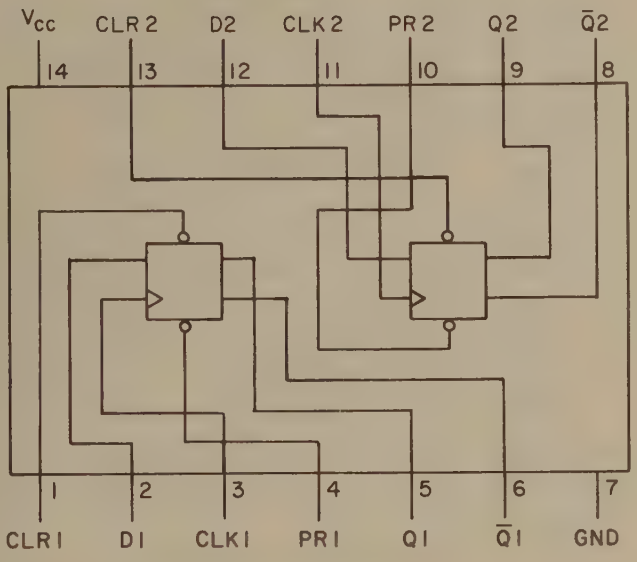


FIGURE 11-26a

TRUTH TABLE

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	$\bar{Q}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1	1
1	1	⌐⌐	1	1	0
1	1	⌐⌐	0	0	1
1	1	0	X	Q_0	$\bar{Q}_0$

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
⌐⌐ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED

FIGURE 11-26b

11.0.27 74LS86 EXCLUSIVE-OR GATE

The 74LS86 is a low power Schottky TTL gate. The 74LS86 performs logically identical to the 4030 but is a faster device. The hi TTL output level may range between +2.0 V to +5.0 V. A lo level will be less than 0.4 V. The pin configuration is different than the 4030 devices.

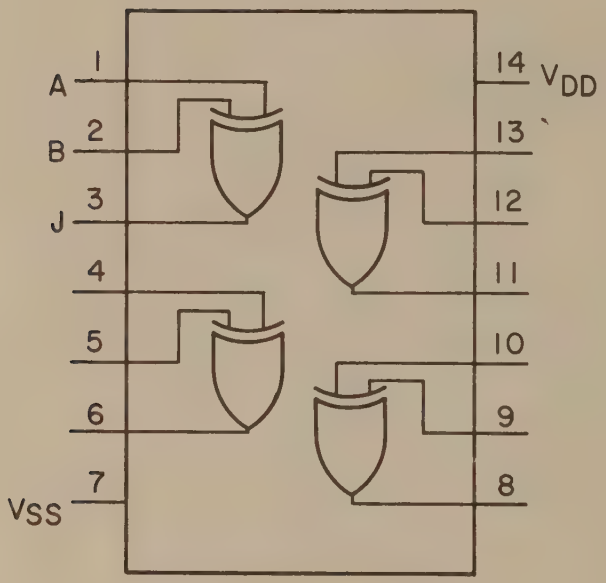


FIGURE 11-27a

TRUTH TABLE

INPUTS A	INPUTS B	OUTPUT J
0	0	0
1	0	1
0	1	1
1	1	0

0 = LO
1 = HI

FIGURE 11-27b

11.0.28 74LS175 QUAD D TYPE FLIP-FLOP

The 74LS175 is a low power Schottky TTL device containing four D type flip-flops. These flip-flops perform in the same manner as 74LS74 flip-flops. All four flip-flops share a common clock input and a common reset (clear) input. A TTL hi level may be +2.0 V to +5.0 V. A lo level will be less than 0.4 V.

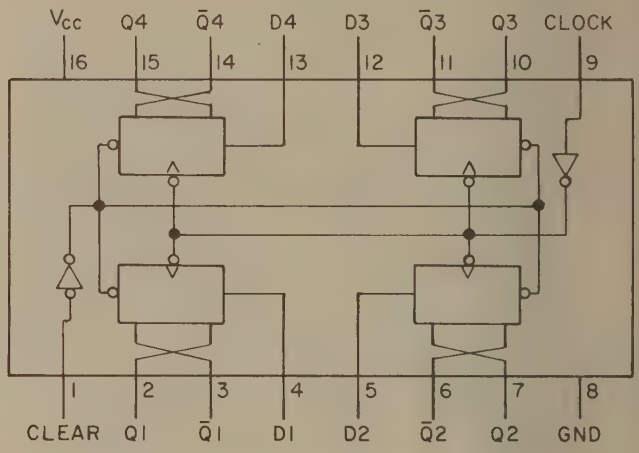


FIGURE 11-28a

TRUTH TABLE

INPUTS CLEAR	INPUTS CLOCK	INPUTS D	OUTPUTS Q	OUTPUTS Q̄
0	X	X	0	1
1	⎍	1	1	0
1	⎍	0	0	1
1	0	X	Q_0	$\bar{Q}_0$

1 = HIGH LEVEL
0 = LOW LEVEL
X = DON'T CARE
⎍ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED

FIGURE 11-28b

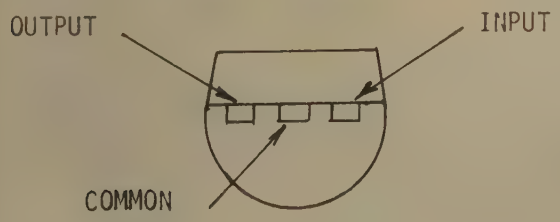
11.1 LINEAR INTEGRATED CIRCUIT DESCRIPTION

The following is a brief functional description of the linear integrated circuits used in the 6040 Selective Level Meter. Where a number of integrated circuits perform the same function, they will be discussed as a group. Unique features making a particular integrated circuit useful in the 6040 will be called out.

11.1.1 THREE TERMINAL POSITIVE REGULATORS

A three terminal regulator converts a varying D.C. input voltage to a fixed constant D.C. output voltage between the circuit output and the common terminal.

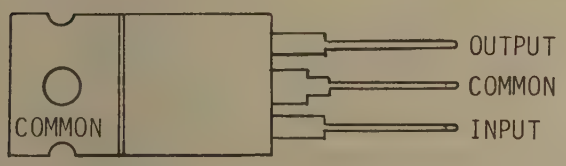
(a) The 78LO5, 78LO8, 78LO10 are regulators having 5.0 V, 8.0 V, and 10.0 V outputs respectively. These regulators have a TO-92 package and have a 100 mA output current capability. A LM340LAZ series regulator may be substituted for a 78L series type.



TO-92 REGULATOR

FIGURE 11-29a

(b) The LM340T-5.0 and LM350T-10.0 have 5.0 V and 10.0 V outputs respectively. These regulators have a TO-220 package and have a 1.0A output current capability. A 78XX series regulator may be substituted for a LM340T series type.



TO-220 REGULATOR

FIGURE 11-29b

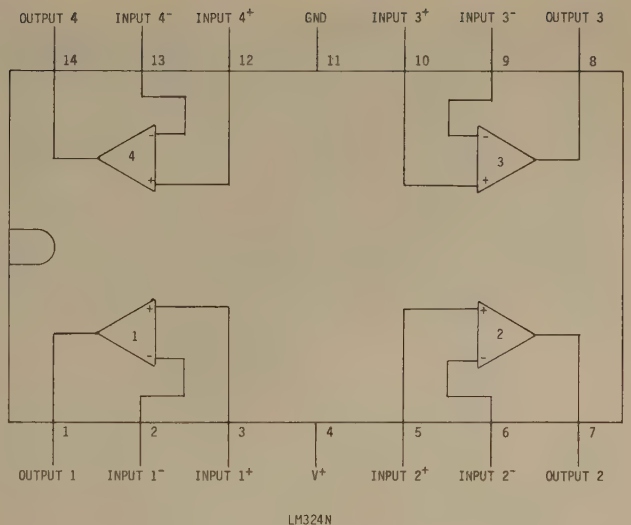
11.1.2 OPERATIONAL AMPLIFIERS

An operational amplifier is a differential amplifier with very high gain and a very high input impedance. A positive transition on the + input will drive the output in a positive direction while a positive transition on the − input will drive the output in a negative direction. Different operational amplifiers are used in the 6040 for performance and economic reasons.

(a) The LM324 and LM358 are bipolar amplifiers with 10 mA output current source capability.

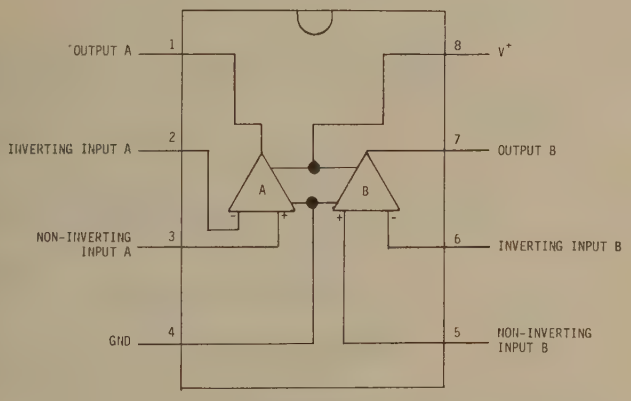
The LM324 is a quad unit with a 14 pin dual-in-line package.

The LM358N is a dual unit with a 8 pin dual-in-line package.



LM324N

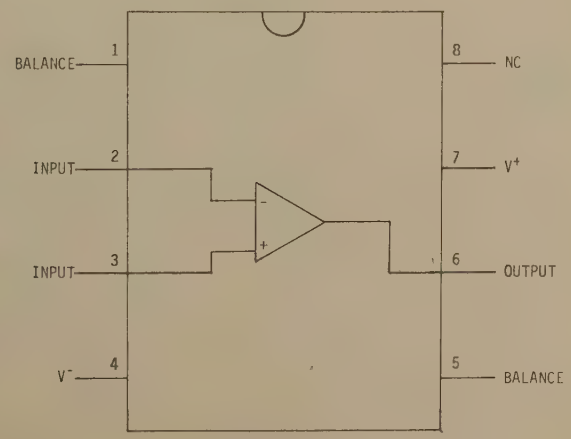
FIGURE 11-30a



LM358N

FIGURE 11-30b

(b) The LF356N and LF357N are BI-FET operational amplifiers. These units have very good noise characteristics making them suitable for use in the low signal level portion of the 6040 I.F. amplifier. The LF357N has a typical gain bandwidth product of 20 MHz allowing it to be employed as an RF amplifier.



LF356N or LF357N

FIGURE 11-30c

11.1.3 VOLTAGE COMPARATORS

A voltage comparator is primarily used to convert analog signals to digital signals. The output will be either HI or LO depending on the relationship between the different inputs. When the + input is more positive than the − input the output is driven HI. When the + input is more negative than the − input the output is driven LO.

(a) The LM393N is a dual voltage comparator with open collector outputs. The outputs require a pull up resistor in order to provide a HI output voltage. This device was used where high precision and high speed were not required.

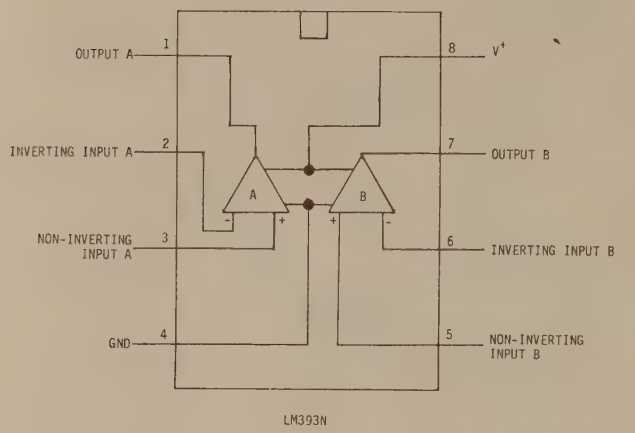


FIGURE 11-31a

(b) The LM311N is a high speed voltage comparator. The balance inputs can be used to adjust the input offset voltage. The output can be taken from either the output transistor collector pin 7, or the output transistor emitter pin 1. For a pin 7 output, pin 1 is connected to ground. For a pin 1 output, pin 7 is connected to V+. When the pin 1 output is used, the input polarities are reversed from those normally shown on the pin diagram.

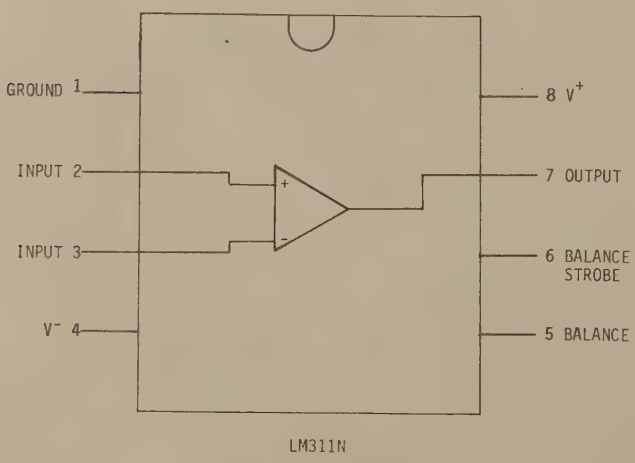


FIGURE 11-31b

11.1.4 LM329BZ

The LM329BZ is an integrated circuit functioning as a highly stable, temperature compensated 6.9 V zener diode. It provides the reference voltage for the 6040 level calibration oscillator. The TO-92 package version is used in the 6040.

BOTTOM VIEW

LM329BZ

FIGURE 11-32a

11.1.5 LM377N

The LM377N is a dual power amplifier. The amplifiers have differential inputs and operate in similar manner to an operational amplifier. In the 6040, the amplifiers are wired in a bridge configuration to drive the unit speaker or an external load.

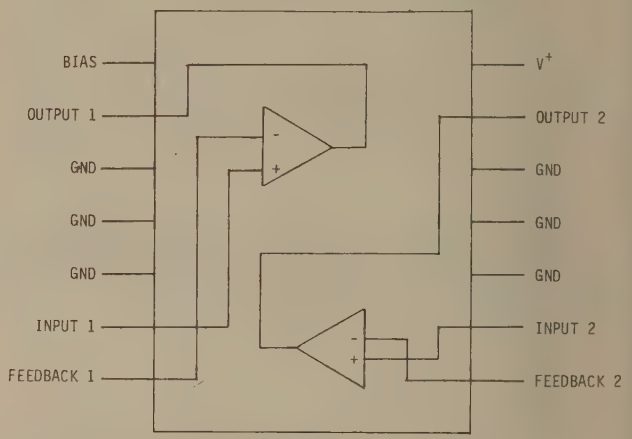


FIGURE 11-33a

11.1.6 MC1350 I.F. AMPLIFIER

The MC1350 is a monolithic I.F. amplifier. The circuit has internally biased differential inputs and open collector or balanced outputs. The outputs are intended to drive the primary winding of a center tapped I.F. transformer. The circuit also has an AGC input, which is used in 6040 units to set I.F. gain.

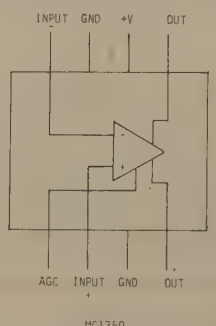


FIGURE 11-34a

CHAPTER 12
SCHEMATIC DIAGRAMS

FIGURE 12-1
INPUT CIRCUITRY SCHEMATIC DIAGRAM

FIGURE 12-2
I.F. AND DEMODULATION SCHEMATIC DIAGRAM

FIGURE 12-3
LOCAL OSCILLATORS SCHEMATIC DIAGRAM

FIGURE 12-4
FREQUENCY CONTROL AND DISPLAY SCHEMATIC DIAGRAM

FIGURE 12-5
LEVEL OUTPUTS AND AUTO/OFF SCHEMATIC DIAGRAM

NOTES INPUT SELECTOR (A2)

1. ALL RESISTORS WITH 0.1% TOLERANCE ARE POWER RATED AT 1 WATT, 70°C COMMERCIAL, 25ppm/°C.

NOTES ATTENUATOR/SUMMING AMP (A3)

1. LATCHING RELAYS K1 THRU K4 ARE ALL SHOWN IN THE "OUT" POSITION (-80 dBm ON LEVEL RANGE SWITCH). ALL 4 SWITCHES INSIDE EACH LATCHING RELAY ARE MECHANICALLY TIED TOGETHER.
2. ALL RESISTORS WITH 0.1% TOLERANCE ARE POWER RATED AT 1/2WATT, 70°C COMMERCIAL, 25ppm/°C.
3. UNLESS OTHERWISE NOTED, ALL CAPACITORS ARE 50 WVDC MIN., 20%, NONPOLAR.

NOTES AUTO RANGING (A19)

1. A TIMING SEQUENCE IS GENERATED WHEN THE 6040 IS TURNED ON, OR WHEN A CHANGE IN THE LEVEL RANGE (MANUAL OR AUTO RANGING) OCCURS; FIRST, A 150 mSEC TIMING DELAY IS GENERATED FOLLOWED BY A 32mSEC 12 VOLT PULSE (V_R) WHICH LATCHES THE 4 RELAYS (K1-K4) IN THE ATTENUATOR (A3) IN THEIR PROPER POSITION (IN/OUT).
2. UNLESS OTHERWISE NOTED, ALL CAPACITORS ARE 50 WVDC, 10%, NONPOLAR.

NOTES: NOISE COMPENSATION (A24)

1. RESISTOR R7 NOT USED ON UNITS WITH SERIAL NO.'S 101-200.
2. BOARD ASSY NO. 110 00151 00 USED ONLY ON UNITS WITH SERIAL NO.'S 101-200.
3. FOR "C" MESSAGE EQUIVALENT NOISE RESPONSE UNITS; R1, R2, R4 & R7 ARE NOT USED. R5 IS 20K, R6 IS 10K.

NOTES: GENERAL

1. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE 5% TOL. 1/4 WATT AT 70°C COMMERCIAL, VALUES IN OHMS.
2. UNLESS OTHERWISE NOTED, ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. REFERENCE DESIGNATIONS ARE ASSIGNED STARTING WITH ONE (1) AT EACH MODULE. TO DEFINE PART AND LOCATION, PREFIX THE REFERENCE DESIGNATION WITH MODULE IDENTIFICATION SUCH AS A2R1. CHASSIS COMPONENTS ARE NOT PREFIXED IN THIS MANNER.
4. ALL ROTARY SWITCHES ARE VIEWED FROM KNOB END AND ARE SHOWN IN THE CCW POSITION. REFER TO INDIVIDUALS FOR THE SCREENING AT EACH POSITION.
5. PANEL CONTROL MARKING DENOTED BY ▭ BOXES.
6. UNLESS OTHERWISE NOTED, ALL RESISTORS WITH 1% TOLERANCE ARE POWER RATED AT 1/8 WATT 125°C COMMERCIAL 100ppm/°C.

RYCOM INSTRUMENTS, INC.

FIGURE 12-1 SCHEMATIC DIAGRAM 6040
TITLE-INPUT CIRCUITRY
DRAWING NO. 032 00124 00

INPUT ASSY (A17)

CALIBRATION OSCILLATOR (A14)
110 00149 00

NOISE COMPENSATION (A24)
110 00151 01/02 (00)

INPUT SELECTOR (A2)
110 00136 00

AUTO RANGING (A19)
110 00144 00

VOLTAGE REGULATOR

GLITCH SWALLOWER

INCREASE / DECREASE ATTEN.

ATTEN. CLOCK

UNBALANCED INPUT

BALANCED INPUT

TO (A1) J5-10 BLK

TO (A1) J5-A RED/BLK

TO (A4) J6-2 RED

TO (A4) J6-3 ORN

TO (A4) J6-1 BRN

TO (A4) J6-4 YEL

TO (A22) WA2

TO S3-6 W/RED

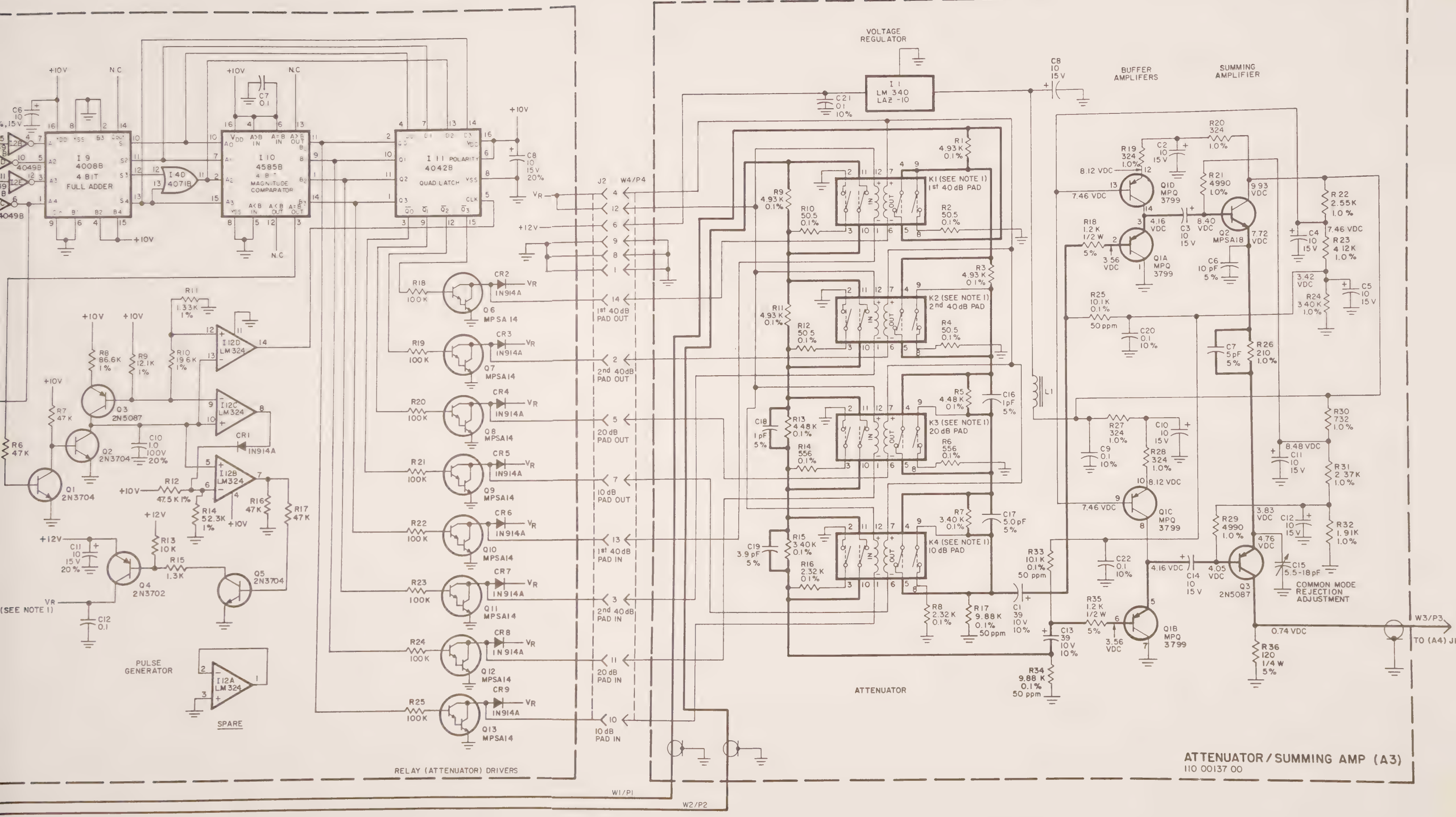
TO S3-12 W/BLK

+10V

+12V

+5V

N.C.


I 9 4008B 4 BIT FULL ADDER
I 10 4585B 4 BIT MAGNITUDE COMPARATOR
I 11 POLARITY 40428 QUAD LATCH
I 40 4071B
I 1 LM 340 LAZ -10
VOLTAGE REGULATOR
BUFFER AMPLIFERS
SUMMING AMPLIFIER
ATTENUATOR
PULSE GENERATOR
SPARE
RELAY (ATTENUATOR) DRIVERS
K1 (SEE NOTE 1) 1st 40dB PAD
K2 (SEE NOTE 1) 2nd 40dB PAD
K3 (SEE NOTE 1) 20dB PAD
K4 (SEE NOTE 1) 10dB PAD
COMMON MODE REJECTION ADJUSTMENT
TO (A4) J1
W1/P1
W2/P2
W3/P3
ATTENUATOR / SUMMING AMP (A3)
110 00137 00

NOTES: POWER SUPPLY (A1)

1. RESISTORS R1 AND R7 HAVE A ±200 PPM/C° T.C.
*2. ( ) RESISTOR VALUES ARE FOR UNITS WITH SN'S 101 TO 200.
*3. R3 REPLACED BY A WIRE ON UNITS WITH SN'S 201 AND ABOVE.
*4. P5 PIN E AND PIN F ARE NOT CONNECTED ON UNITS WITH SN'S 201 AND ABOVE.
5. BOARD ASSY NO. 110 00150 (00) USED ONLY ON UNITS WITH SERIAL NO.'S 101 TO 200.

NOTES: I.F. (A4)

1. ALL 0.1% TOLERANCE RESISTORS ARE POWER RATED AT 1/2 WATT, 70°C-COMMERCIAL RATING, 50 ppm/°C MAX.
2. ALL 1% TOLERANCE RESISTORS ARE POWER RATED AT 1/8 WATT, 125°C-COMMERCIAL RATING, 100 ppm/°C MAX.
3. ALL VARIABLE RESISTORS ARE 10% TOLERANCE, 1/2 WATT, 70°C-COMMERCIAL RATING, 100 ppm/°C MAX.
4. ALL RESISTORS NOT MARKED WITH TOLERANCE ARE 5%, 1/4 WATT, 70°C-COMMERCIAL RATING.
5. UNLESS OTHERWISE NOTED, ALL CAPACITOR VALUES ARE IN MICROFARADS (uF), 50 W VDC, 10%, NON-POLAR
6. ALL CAPACITORS MARKED IN PICO-FARADS ARE 5% TOLERANCE MAX., 100 W VDC.
7. A4Q3 IS A SELECTED PART. SEE PARTS LIST FOR PART NO.

NOTES: GENERAL

1. UNLESS OTHERWISE NOTED, ALL RESISTOR VALUES ARE IN OHMS.
2. UNLESS OTHERWISE NOTED, ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. REFERENCE DESIGNATIONS ARE ASSIGNED STARTING WITH ONE (1) AT EACH MODULE. TO DEFINE PART AND LOCATION, PREFIX THE REFERENCE DESIGNATION WITH MODULE IDENTIFICATION SUCH AS (A4) R1. CHASSIS COMPONENTS ARE NOT PREFIXED IN THIS MANNER.
4. ALL ROTARY SWITCHES ARE VIEWED FROM KNOB END AND ARE SHOWN IN THE CCW POSITION. REFER TO INDIVIDUALS FOR THE SCREENING AT EACH POSITION.
5. PANEL CONTROL MARKING DENOTED BY ▭ BOXES.
*6. ASTERISK IS USED TO INDICATE A CHANGE AT SN 201.

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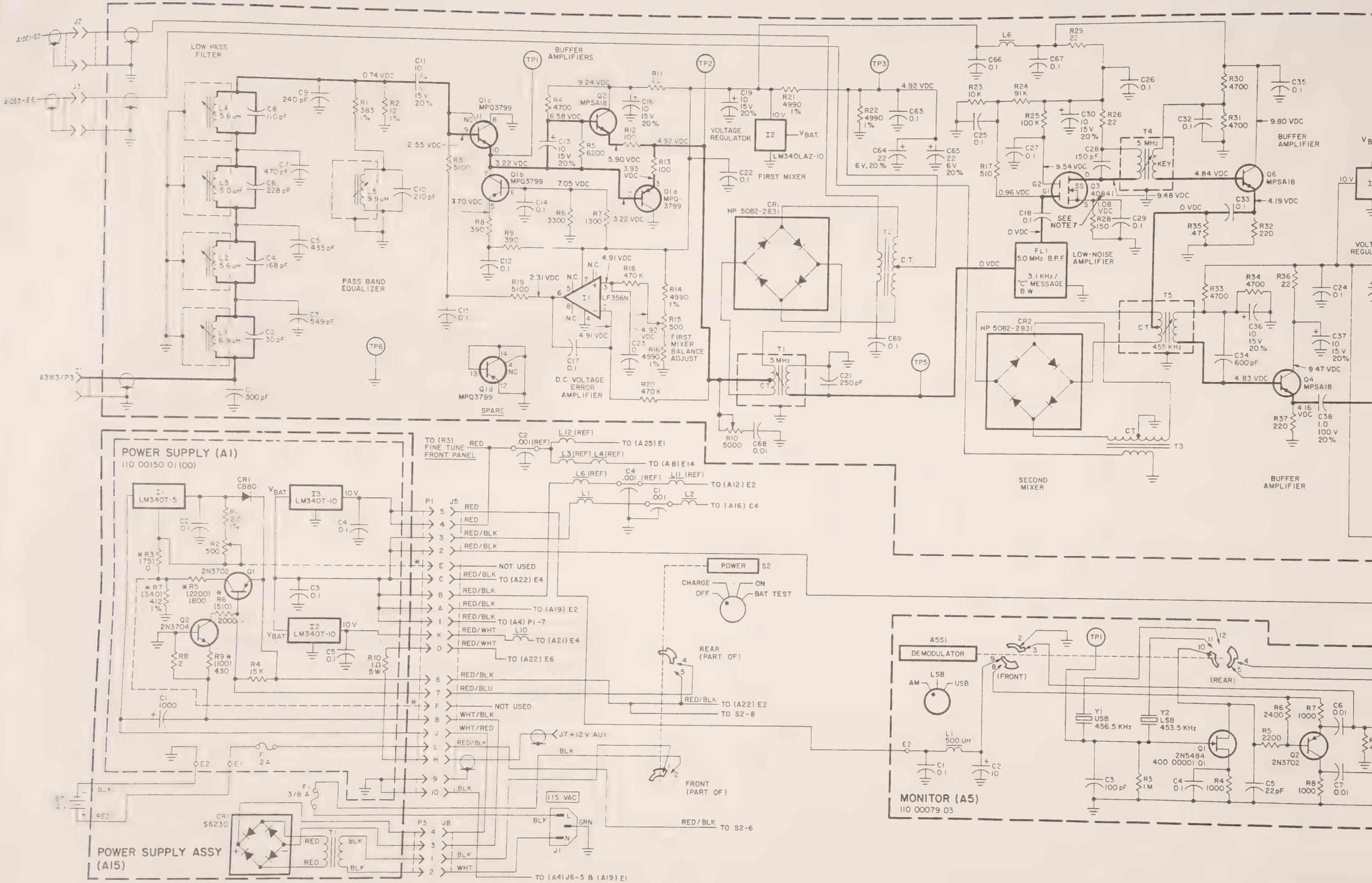
FIGURE 12-2 SCHEMATIC DIAGRAM 6040
TITLE-I.F. AND DEMODULATION
DRAWING NO. 032 00125 00 REV. C


LOW PASS FILTER
BUFFER AMPLIFIERS
PASS BAND EQUALIZER
D.C VOLTAGE ERROR AMPLIFIER
SPARE
VOLTAGE REGULATOR
FIRST MIXER
FIRST MIXER BALANCE ADJUST
LOW-NOISE AMPLIFIER
SECOND MIXER
BUFFER AMPLIFIER
POWER SUPPLY (A1)
110 00150 01 (00)
POWER SUPPLY ASSY (A15)
MONITOR (A5)
110 00079 03
DEMODULATOR
FRONT (PART OF)
REAR (PART OF)
TO (R3) FINE TUNE FRONT PANEL
TO (A25) E1
TO (A8) E14
TO (A12) E2
TO (A16) C4
TO (A19) E2
TO (A4) P1-7
TO (A21) E4
TO (A22) E6
TO (A22) E4
TO S2-8
TO S2-6
TO (A4) J6-5 & (A19) E1
J7 +12 V AUX
115 VAC
POWER S2
CHARGE
OFF
ON
BAT TEST
A3W3/P3
A1DE1-E2
A2E5-E6
LM340LAZ-10
LF356N
MPQ3799
MPSA18
2N3702
2N3704
2N5484
400 00001 01
S6230
HP 5082-2831
LOW-NOISE AMPLIFIER
3.1 KHz / "C" MESSAGE BW
5.0 MHz B.P.F.
SEE NOTE 7
KEY
LSB
USB
AM
Y1 USB 456.5 KHz
Y2 LSB 453.5 KHz
455 KHz
5 MHz
0.74 VDC
9.24 VDC
6.58 VDC
2.55 VDC
3.22 VDC
5.90 VDC
3.93 VDC
7.05 VDC
7.70 VDC
4.91 VDC
2.31 VDC
4.92 VDC
4.49 VDC
4.92 VDC
9.80 VDC
9.54 VDC
0.96 VDC
9.48 VDC
4.84 VDC
4.19 VDC
0 VDC
10.8 VDC
9.47 VDC
4.83 VDC
4.16 VDC

INPUT-IMPEDANCE POWER-TO-VOLTAGE LEVEL-CORRECTION SWITCHABLE ATTENUATOR

I5 40678 16:1 ANALOG MULTIPLEXER

R38 49.9,0.1% 50Ω BRG. R39 226,1% R40 49.9,0.1% 75Ω BRG. R41 226 0.1% R42 54.9K 1% R43 49.9,0.1% 75Ω R44 221 0.1% R45 9760 1% TERM/CAL R46 634,0.1% 124Ω BRG. R47 113 0.1% R48 287K 1% R49 64.9,0.1% 124Ω TERM R50 113 0.1% R51 7870 1% R52 66.5,0.1% 135Ω BRG. R53 107 0.1% R54 8450 1% R55 68.1,0.1% 135Ω TERM. R56 105 0.1% R57 24.3K 1% R58 69.8,0.1% 150Ω BRG. R59 100 0.1% R60 4120 1% R61 71.5,0.1% 150Ω TERM. R62 97.6 0.1% R63 8870 1% R64 137,0.1% 600Ω BRG. R65 8250,1% R66 59.0,0.1% R67 143,0.1% 600Ω TERM R68 294K,1% R69 57.6,0.1% CAL

COMMON OUT/IN V_{DD} V_{SS} INHIBIT

0/10 VDC

R70 47K R71 47K R72 47K R73 47K R74 22

C44 10 15V 20% C45 0.1

R75 47K C46 0.1 R76 1MEG C47 10 15V 20% R77 1MEG R78 22 R79 300 C48 0.1 R80 1800 C49 10 15V 20% R81 464 1% R82 732 1% R83 200 R84 270 R85 560 R86 180 R87 47K R90 22 C51 10 15V 20% C20 0.1

FL2 455KHz B.P.F. 50/100 Hz B.W.

FL3 455KHz B.P.F. 10 KHz B.W.

WIDE/NARROW FILTER EQUALIZER ADJUSTMENT

WIDE/NARROW SELECTION CIRCUIT

I6 LF357N BUFFER AMPLIFIER

I7a I7b I7c I7d 4066

I8a I8b I8c I8d 4066

V_{BAT}

R93 22 R94 22 C53 10,15V 20% C54 0.1 C57 10,15V 20% C55 0.1 C56 0.1 C52 0.1 C50 0.1 R88 1MEG R89 1MEG R91 300 R92 1800 R96 20K R97 10K R98 15K R99 18K R100 1000 R101 22 R102 51 R103 68K R104 3900 R105 4700 R106 3900 R107 3300 R108 100K C58 500pF C59 0.1 C60 0.1 C61 0.1 C62 10 15V 20% C40 0.1 C41 0.1 C42 0.1 C43 0.1 C31 0.1

I9 LF357N CAL LEVEL VAR GAIN AMPLIFIER

I10 MC1350P

T6 455 KHz C.T.

THERMAL CONNECTION

BUFFER AMPLIFIER

CAL. LEVEL CENTER ADJUSTMENT

TRIFILAR WIRE

TEMPERATURE/GAIN COMPENSATION

OUTPUT AMPLIFIER

Q5 MPSA18 Q7 2N4124 Q8 2N5087 CR3 IN914A TP4

9.80 VDC 9.60 VDC 4.89 VDC 3.23 VDC 4.84 VDC 9.81 VDC 5.80 VDC 5.17 VDC 1.07 VDC 0.39 VDC 9.79 VDC 4.88 VDC 4.88 3 VDC 9.88 VDC 0 VDC

J4 P6 J6

RED L15 TO (A2) S2CR-5 & 8

ORN L16 TO (A2) S2CR-3 & 9

BRN L14 TO (A2) S2CF-6

YEL L13 TO (A2) S2CF-7

SLT TO CAL LEVEL, R2

S3 (SELECTIVITY) (PART OF)

BLU BLK WHT

RED/BLK BLK

L9 TO (A1) J5-1 TO (A1) J5-10

I.F. (A4) 110 00138 00/03

TO (A8) E6

E15 E16 E7 E8 E10 E11 E3 E12 E13 E9

R4 25K LEVEL GRN W/GRN

R11 10K R12 3900 R13 1M R14 5600 R15 100K R16 1M R17 47 R10 4700 C8 0.01 C9 0.01 C10 10 C11 22 C12 22

CR1 IN277 CR2 IN277

I2A I2B LM377

OUTPUT J2 V10 V10/W W/V10 LS1

NOTES: 1st L.O. (A9)

1. REMOVED

2. R14 IS INSTALLED ONLY WHEN REQUIRED.

NOTES: GENERAL

1. UNLESS OTHERWISE NOTED, RESISTOR VALUES ARE IN OHMS.
2. UNLESS OTHERWISE NOTED, CAPACITOR VALUES ARE IN MICROFARADS.
3. REFERENCE DESIGNATIONS ARE ASSIGNED STARTING WITH ONE (1) AT EACH MODULE. TO DEFINE PART AND LOCATION, PREFIX THE REFERENCE DESIGNATION WITH MODULE IDENTIFICATION SUCH AS A9R1. CHASSIS COMPONENTS ARE NOT PREFIXED IN THIS MANNER.
4. ALL ROTARY SWITCHES ARE VIEWED FROM KNOB END AND ARE SHOWN IN THE CCW POSITION. REFER TO INDIVIDUALS FOR THE SCREENING AT EACH POSITION.
5. PANEL CONTROL MARKING DENOTED BY ▭ BOXES.

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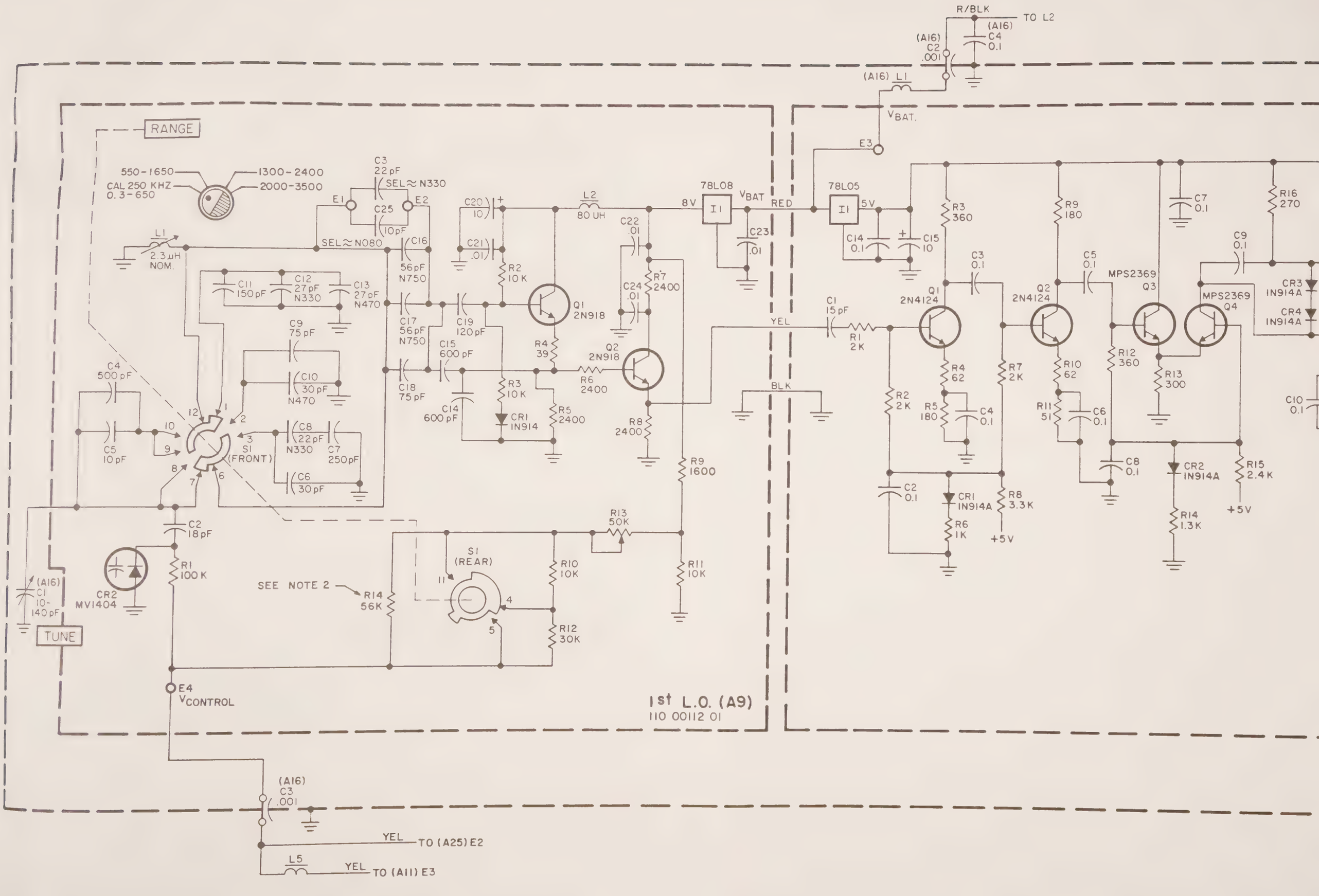
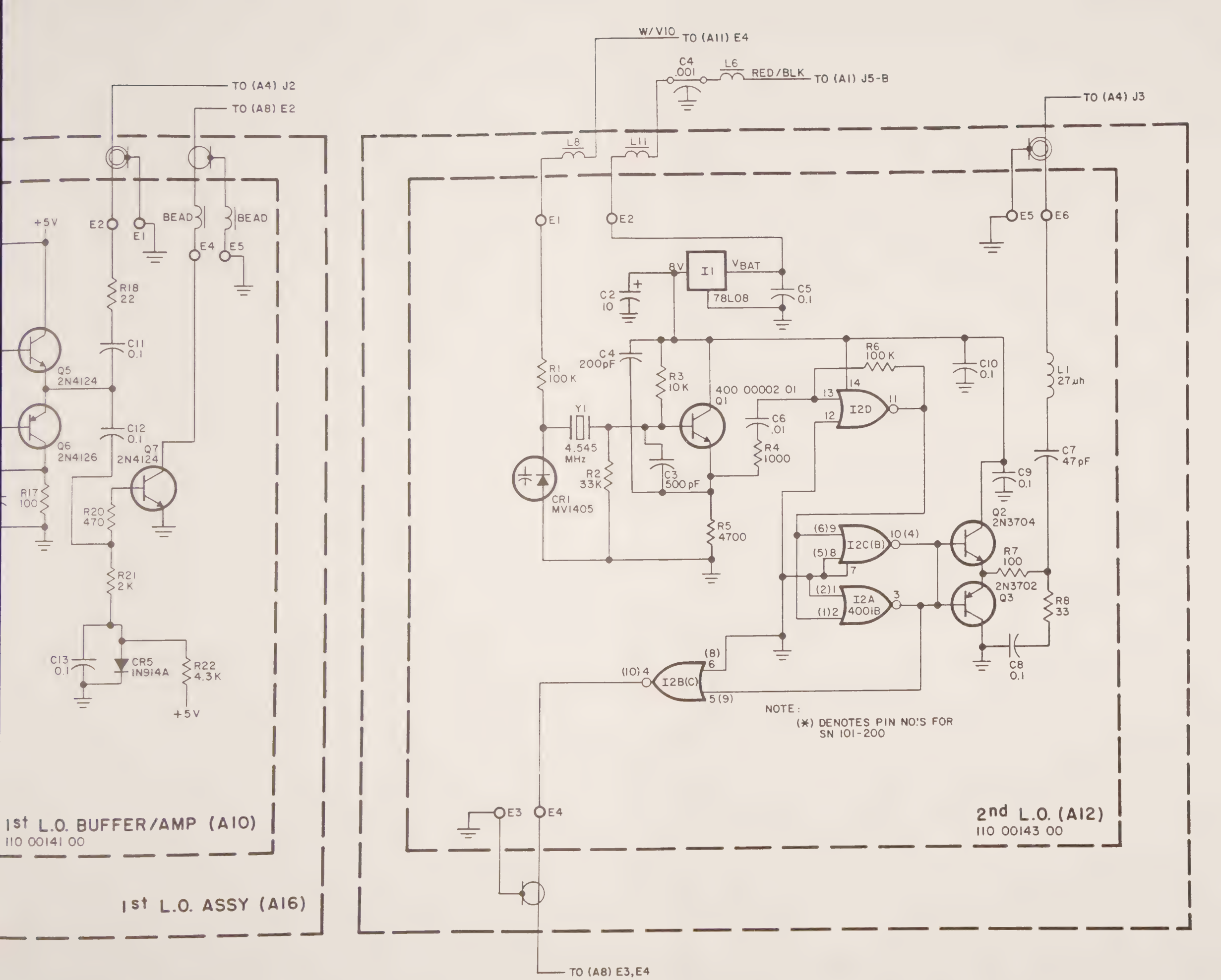
FIGURE 12-3 SCHEMATIC DIAGRAM 6040
TITLE-LOCAL OSCILLATORS
DRAWING NO. 032 00126 00 REV. E



1st L.O. (A9)
110 00112 01


TO (A4) J2
TO (A8) E2
+5V
E2
E1
BEAD
BEAD
E4
E5
R18
22
C11
0.1
Q5
2N4124
C12
0.1
Q6
2N4126
Q7
2N4124
R17
100
R20
470
R21
2K
C13
0.1
CR5
IN914A
R22
4.3K
+5V
1st L.O. BUFFER/AMP (A10)
110 00141 00
1st L.O. ASSY (A16)
W/V10
TO (A11) E4
C4
.001
L6
RED/BLK
TO (A1) J5-B
TO (A4) J3
L8
L11
E1
E2
E5
E6
8V
I1
VBAT
78L08
C2
10
C5
0.1
C4
200pF
R1
100K
R3
10K
400 00002 01
Q1
Y1
4.545
MHz
CR1
MV1405
R2
33K
C3
500pF
R5
4700
C6
.01
R4
1000
R6
100K
C10
0.1
L1
27µh
C7
47pF
C9
0.1
Q2
2N3704
R7
100
2N3702
Q3
R8
33
C8
0.1
I2D
I2C(B)
I2A
4001B
I2B(C)
NOTE:
(*) DENOTES PIN NO:S FOR
SN 101-200
E3
E4
TO (A8) E3,E4
2nd L.O. (A12)
110 00143 00

NOTES: PHASE LOCK LOOPS (A11)

1. POWER & GROUND CONNECTIONS:
   +10V PIN 16; GND. PIN 8; I1, I4, I5, I8 AND I9.
   +10V PIN 14; GND. PIN 7; I2, I3, I6 AND I10.
   +10V PIN 4; GND. PIN 11; I7 (SN 101 TO 200).
   +10V PIN 14; GND. PIN 7; I7 (SN 201 AND ABOVE).
2. BOARD ASSY NO. 110 00142 (00) USED ONLY ON UNITS WITH SERIAL NO.'S 101 TO 200.
3. I7 ( ) PIN-OUTS USED WITH 74C73 ONLY ON UNITS WITH SERIAL NO.'S 101 TO 200.

NOTES: TIMING/COUNTER INPUT (A8)

1. POWER & GROUND CONNECTIONS:
   +10V PIN 16; GND PIN 8; I1, I2, I3, I5, I12, I13, I14, I18, I24 AND I28.
   +10V PIN 14; GND. PIN 7; I4, I6, I7, I8, I10, I11, I15, I16, I17, I21, I25, I26 AND I27.
   +10V PIN 4; GND. PIN 11; I9 (SN 101 TO 200).
   +10V PIN 14; GND. PIN 7; I9 (SN 201 AND ABOVE).
   +5V PIN 16; GND. PIN 8; I23.
   +5V PIN 14; GND. PIN 7; I20 AND I22.
2. I27C PIN 10; SIGNAL COUNT $F = \frac{\text{1st L.O.} - \text{2nd L.O.} - \text{2nd I.F.}}{2}$
   OR
   PASS BAND $F = \frac{\text{1st L.O.} - \text{2nd L.O.} - 445\ \text{KHz}}{2}$
3. I21B PIN 4; $F = \frac{\text{1st L.O.} - \text{2nd L.O.}}{2}$
4. WHEN USED (R12) MAY BE CONNECTED TO EITHER GND A OR +10V B.
5. BOARD ASSY NO. 110 00140 (00) USED ONLY ON UNITS WITH SERIAL NO.'S 101 TO 200.
6. I9 ( ) PIN-OUTS USED WITH 74C73 ONLY ON UNITS WITH SERIAL NO.'S 101 TO 200.

NOTES: FREQUENCY DISPLAY (A7)

1. POWER & GROUND CONNECTIONS:
   +10V PIN 14; GND. PIN 7; I9 AND I10.

NOTES: GENERAL

1. UNLESS OTHERWISE NOTED, ALL RESISTOR VALUES ARE IN OHMS.
2. UNLESS OTHERWISE NOTED, ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. REFERENCE DESIGNATIONS ARE ASSIGNED STARTING WITH ONE (1) AT EACH MODULE. TO DEFINE PART AND LOCATION, PREFIX THE REFERENCE DESIGNATION WITH MODULE IDENTIFICATION SUCH AS A1IR1. CHASSIS COMPONENTS ARE NOT PREFIXED IN THIS MANNER.
4. PANEL CONTROL MARKING DENOTED BY ▭ BOXES.

RYCOM INSTRUMENTS, INC.

FIGURE 12-4 SCHEMATIC DIAGRAM 6040
TITLE - FREQUENCY CONTROL AND DISPLAY
DRAWING NO. 032 00127 00 REV. C

LOW PASS FILTER (A25)
110 00153 00

PHASE LOCK LOOPS (A11)
110 00142 01 (00)

* FREQUENCY PRESENT ONLY WHEN AFC ACTIVE

TO C2
L12
RED
E1
C1 0.1
R1 470K
C2 0.1
R2 240K
R3 160K
C4 0.1
C3 0.1
E2
I1A
I1B 358
YEL
W/ORN
TO (A16) C3
L5(REF)
AFC
TO (A21) E11
ORN
W/GRN
OFF
S4
6.5V-7.5V
E3
1st L.O. CONTROL
E1
LOCK ENABLE
L7
C3 .001
W/V10
C5 0.1
R3 10K FINE TUNE
RED
V10/W
E2
FINE TUNE
R3 10K
+10V
R4 270K
C4 22
C3 0.1
R1 47 M
C1 10
C2 0.22
I10D
R7 392 K 1%
R2 392 K 1%
R8 20K
I6A 4013B
I6B 4013B
I10A 4030B
625 Hz
I3B 4013B
I4B 4518B CK
I2A 4023B
I2C
* 1.25 KHz
* 625 Hz
I5B 4520B
* 5.00 KHz
I4A 4518B CK
MY1 TCXO 4,450 KHz
C6 0.1
C7 0.1
C8 10
C9 0.1
C10 0.1
C11 10
5.00 KHz
505 KHz
I10C
I7B
I8B 4015B
I3A 4013B
I8A 4015B
I9B 4518B
I9A 4518B CK
I10B
R5 200 K
C5 0.22
E4 3.5V-5.5V
2nd L.O. CONTROL
TO (A12) E1
W/V10
312.5 Hz
I5A 4520B CK
I1A 4518B CK
I2B
74C107 (74C73)
I7A
I1B 4518B CK
445 KHz IN
455 KHz 2ND IF IN
4.545 MHz IN
P1 J1
8
5
7
6
1
4
3
2
L4 L3 C4 .001
TO (A1) J5-4
4.45 MHZ
TP1
BLK E13
RED E14
+10V
74C107 (74C73)
I9A CK
I10B
I9B CK
I8B
I1A 4013 CK
I1B 4013 CK
I12B CK
I4B 4085B
W/ORN E11
RED/W E17
C6,C8, C10 10
C7, C9, C11, C12, C14, C15, C18 0.1
R13 30K
I10D
312.5 Hz
NO LOCK
I18A CK 4520B
I18B CK
I13 CK 4017B
I14 4020B
I12A 4518B CK
I15A 4013B CK
TO (A21) E5,E6
E8 4.45KHz OUT
E7
I21D
SIG. CNT.
RED/W
DISPLAY
SIGNAL COUNT
1 Hz
10 Hz
BLK
S5
CENTER PASS BAND
E12 W/BLU
I24 4017B
I25B 4085B
I26B
I25A 4085B
I27D
COUNT
I27C
SEE NOTE 3
445KHz OUT
455KHz 2ND I.F. OUT
TO (A5) E15,E16
E6 2ND I.F. IN
E5
C2 .01
R6 10K
I19A LM393
R9 4.7K
TO (A21) E1,E2
E10 2ND I.F. OUT
E9
C3 .1
R16 1.1K
I20B
TO (A10) E4,E5
BEAD
E2 1ST L.O. IN
E1
2N3704 Q1
R2 30 K
R1 20 K
C16 22 pF
R3 820
74LS74 I22A
2.2725 MHz
I29 78L05 5V REG
4.545MHZ OUT
TO (A12) E3,E4
E4 2ND L.O. IN
E3
C1 .01
R5 100 K
I21A 4001B
I19B
I20A 74LS86
I20D
I22B CK S
SPARE

NOTE
SEE FIGURE 6-5 FOR FREQUENCY COUNTER CONTROL SIGNAL TIMING.

M.R.
L.E
GATED COUNT
DEC. PT. 3
DEC. PT. 2
DIS 2
SIG CNT
1000
AFC
SCAN
LCD CLOCK
L.O. DIFF
312.5 Hz
+10V
+5V
W/BLU E15
RED/BLU E16
TO (A22) E5
TO (A22) E3
SEE NOTE 4
SEE NOTE 3
(AFC)
(SIGNAL COUNT)
DP2
DP3
B.P.
6-DIGIT LCD
430 00098 00

I1 4553B
I2 4553B
I3 4543B
I4 4543B
I5 4543B
I6 4543B
I7 4543B
I8 4543B
I11

I4A 4085B
I5B
I5A 4518B
I6C
I7A 4013B
I8D
I8C
I8A 4001B
I6B 4023B
I9B
I9C
I9D
I9A 4001B
I10A 4011B
I16B
I7B
I17 B
I17A 4013B
I6A 4023B
I10C
I5B
I16A 4013B
I10A 4030B
I10C
I10D
I10B
I26A 4013
I27B
I27A 4030B
I21C
I28D
I28A
I28B
I28C
I28 74C175
I20C 74LS86
I21B
I23D
I23A
I23C
I23B
I23 74LS175

R14 1M
C5 0.1
R15 30K
R1 100K
C1 0.1
C2 0.1
R12 100K
R11 30K
C4 .01
R10 1K
DH1

P1 J1
P2 J2

TIMING/COUNTER INPUT (A8)
110 00140 01 (00)

FREQUENCY DISPLAY (A7)
110 00139 00

NOTES: LEVEL DETECTOR (A21)

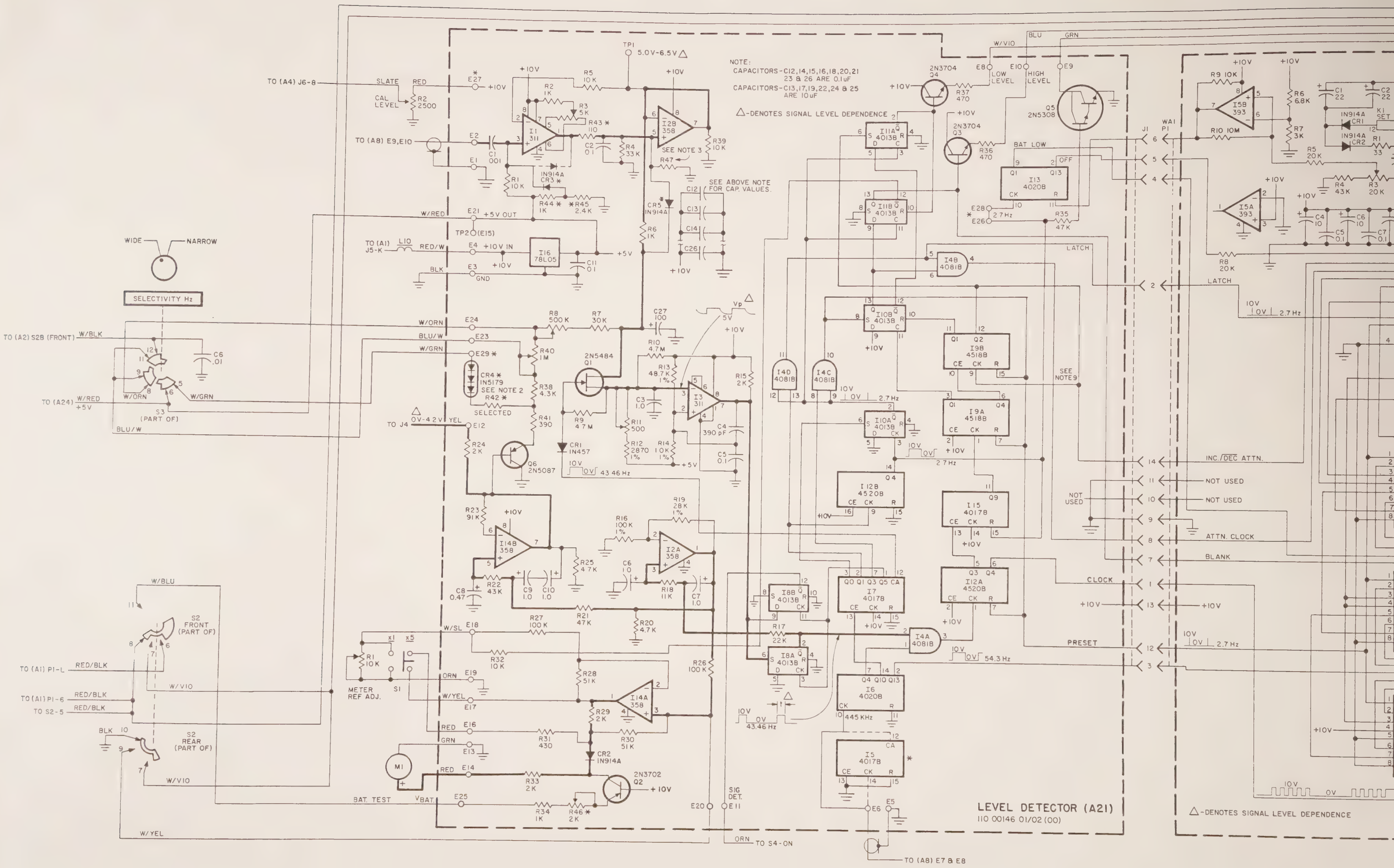
1. C3 HAS A METALLIZED POLYSULFONE DIELECTRIC WHICH PROVIDES A +18ppm/°C T.C. BETWEEN 0°C TO 150°C. R12 HAS A +0-50ppm/°C.
2. R42 AND CR4 ARE INSTALLED ONLY AS REQUIRED.
3. R47 IS USED AS REQUIRED ON UNITS HAVING A "C" MESSAGE EQUIVALENT NOISE RESPONSE.
*4. I5 IS NOT USED ON UNITS WITH SN'S 201 AND UP.
*5. ON UNITS WITH SN'S 101-200, E26-E29, R43-R46 AND CR5 WERE NOT USED.
*6. ON UNITS WITH SN'S 101-200, R4 WAS 100K AND BOARD ASSY NO. WAS 110 00146 00.
*7. ON UNITS WITH SN'S 101-200, CR3 ANODE WAS CONNECTED TO I1-3 & CATHODE TO I1-1. CR4 WAS LOCATED ON S3 AND DESIGNATED CR1.
*8. ASTERISK IS USED TO INDICATE A CHANGE AT SN 201. SEE NOTES 4, 5, 6, & 7.
9. ON UNITS WITH SN'S 101-300, I9-9 WAS CONNECTED TO GROUND.

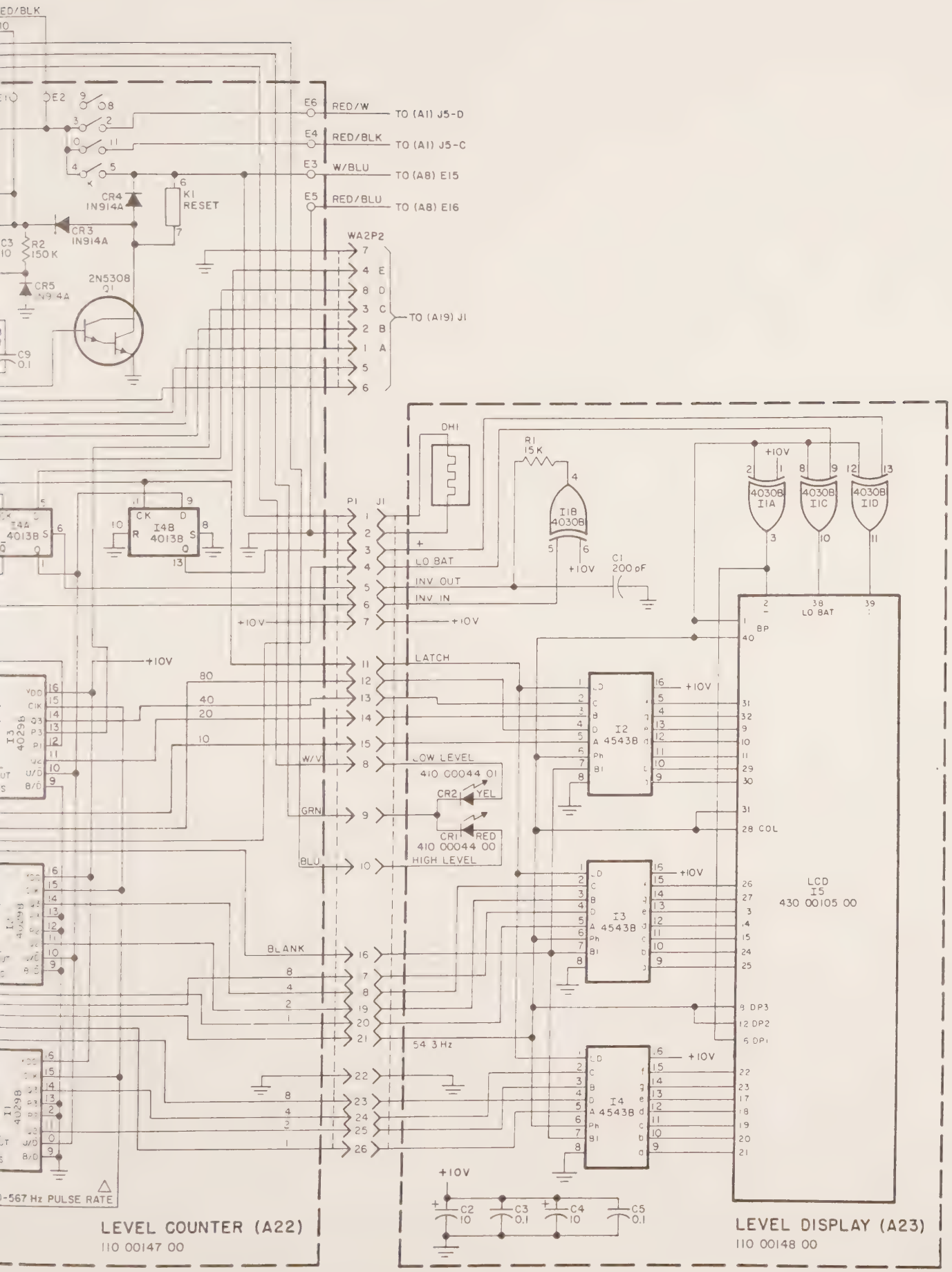
NOTES: GENERAL

1. UNLESS OTHERWISE NOTED, RESISTANCE VALUES ARE IN OHMS.
2. UNLESS OTHERWISE NOTED, CAPACITANCE VALUES ARE IN MICROFARADS.
3. REFERENCE DESIGNATIONS ARE ASSIGNED STARTING WITH ONE (1) AT EACH MODULE. TO DEFINE PART AND LOCATION, PREFIX THE REFERENCE DESIGNATION WITH MODULE IDENTIFICATION SUCH AS A21R1. CHASSIS COMPONENTS ARE NOT PREFIXED IN THIS MANNER.
4. ALL ROTARY SWITCHES ARE VIEWED FROM KNOB END AND ARE SHOWN IN THE CCW POSITION. REFER TO INDIVIDUALS FOR THE SCREENING AT EACH POSITION.
5. PANEL CONTROL MARKING DENOTED BY ▭ BOXES.

RYCOM INSTRUMENTS, INC.

FIGURE 12-5 SCHEMATIC DIAGRAM 6040
TITLE-LEVEL OUTPUTS AND AUTO/OFF
DRAWING NO. 032 00128 00 REV B


NOTE:
CAPACITORS-C12,14,15,16,18,20,21 23 & 26 ARE 0.1uF
CAPACITORS-C13,17,19,22,24 & 25 ARE 10uF
△-DENOTES SIGNAL LEVEL DEPENDENCE
SEE ABOVE NOTE FOR CAP. VALUES.
SEE NOTE 3
SEE NOTE 9
SELECTED
METER REF ADJ.
LEVEL DETECTOR (A21)
110 00146 01/02 (00)
△-DENOTES SIGNAL LEVEL DEPENDENCE
TO (A4) J6-8
TO (A8) E9,E10
TO (A1) J5-K
TO (A2) S2B (FRONT)
TO (A24)
TO J4
TO (A1) P1-L
TO (A1) P1-6
TO S2-5
TO S4-ON
TO (A8) E7 & E8
SELECTIVITY Hz
WIDE
NARROW
CAL LEVEL
SLATE
RED
BAT. TEST
SIG DET.
INC./DEC ATTN.
NOT USED
ATTN. CLOCK
BLANK
CLOCK
PRESET
LATCH
LOW LEVEL
HIGH LEVEL
BAT LOW
OFF
+5V OUT
+10V IN
GND
2.7Hz
54.3Hz
43.46Hz
445KHz


E6 RED/W TO (A11) J5-D
E4 RED/BLK TO (A11) J5-C
E3 W/BLU TO (A8) E15
E5 RED/BLU TO (A8) E16
K1 RESET
CR4 IN914A
CR3 IN914A
R2 150K
CR5 IN914A
2N5308 Q1
C9 0.1
WA2P2
TO (A19) J1
P1 J1
DH1
R1 15K
I18 4030B
C1 200 pF
LO BAT
INV OUT
INV IN
+10V
LATCH
80
40
20
10
W/V
GRN
BLU
BLANK
8
4
2
1
54.3 Hz
LOW LEVEL
410 00044 01
CR2 YEL
CR1 RED
410 00044 00
HIGH LEVEL
I44 4013B
I48 4013B
I3 4029B
I1 4029B
I3 40296
0-567 Hz PULSE RATE
LEVEL COUNTER (A22)
110 00147 00
40308 I1A
40308 I1C
40308 I1D
I2 4543B
I3 4543B
I4 4543B
BP
28 COL
LO BAT
LCD I5
430 00105 00
8 DP3
12 DP2
5 DP1
C2 10
C3 0.1
C4 10
C5 0.1
LEVEL DISPLAY (A23)
110 00148 00